

Introduction

Introduction to Design Methodologies

- The VLSI Design Problem
- Hierarchy and Abstraction
- Synthesis, Analysis, Verification, ...
- Implementation Methods

Quick Tour of EDA tools

- Rough classification

The VLSI Design Problem

Realize a given specification on silicon, optimizing the following features:

- area (yield)
- power dissipation
- speed
- design time
- testability

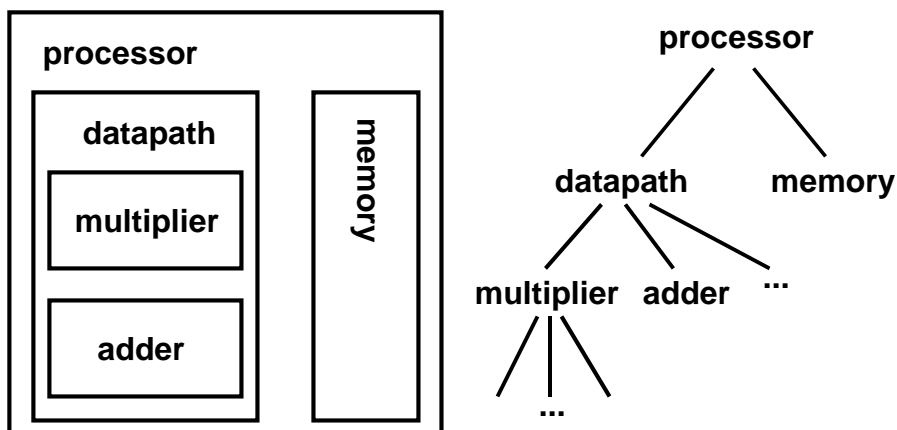
Optimization cannot be done in one step → partition problem and optimize subproblems.

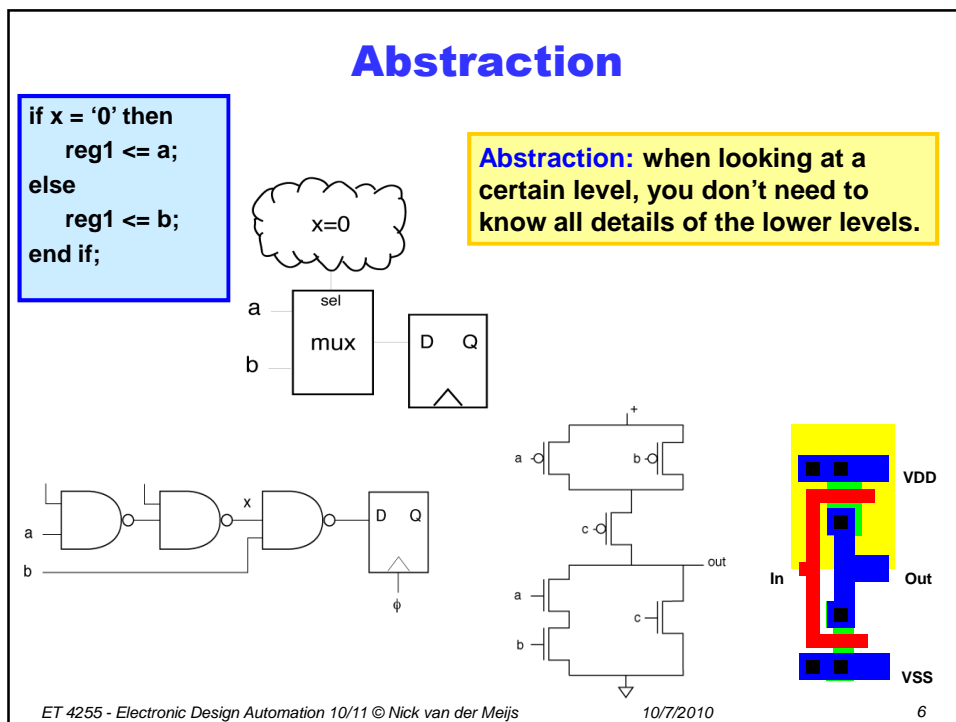
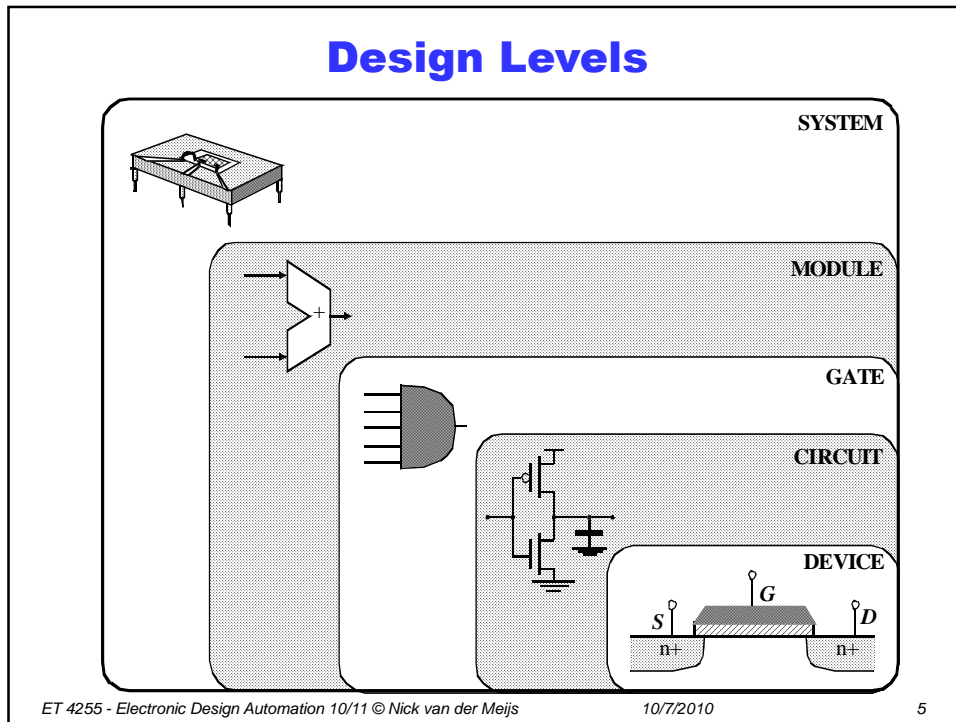
Anonymous Transistors

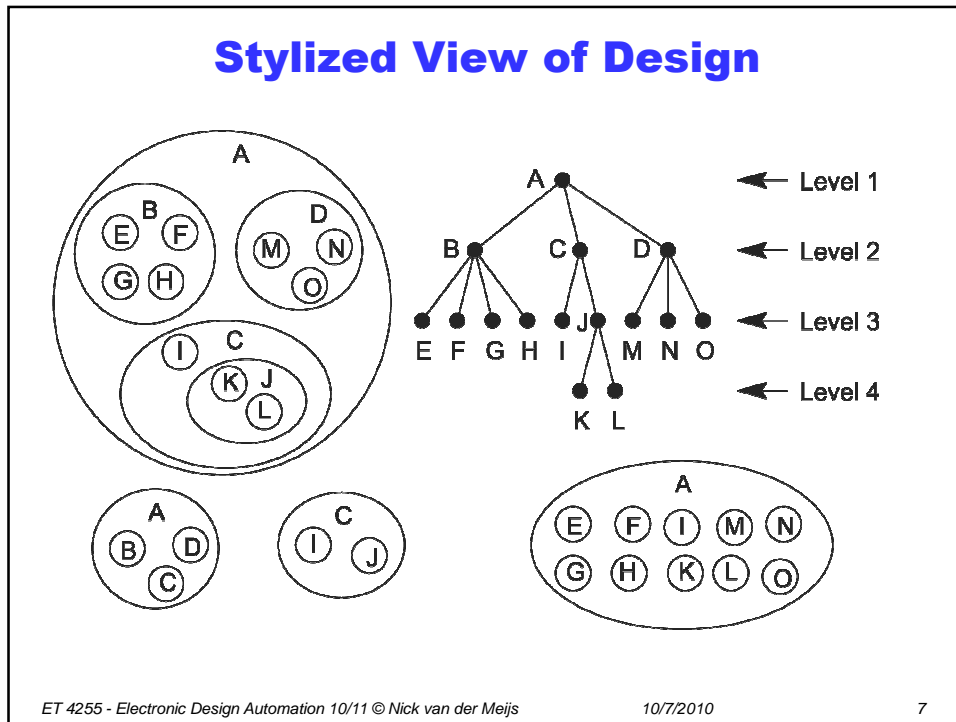
- Large Chips have $\gg 10^8$ transistors
- Cannot consider each transistor separately during design
- Large chips have many “anonymous transistors”
Assembled from pre-designed building blocks
 - Such as on chip memory blocks
 - Or other blocks ranging from adders to complete sub systems [e.g. MP3 decoder, memory, ...]
- Blocks are assembled from sub blocks, and so on
- Block types depend on architecture

Hierarchy (Modularity)

Hierarchy: Something is composed of simpler things







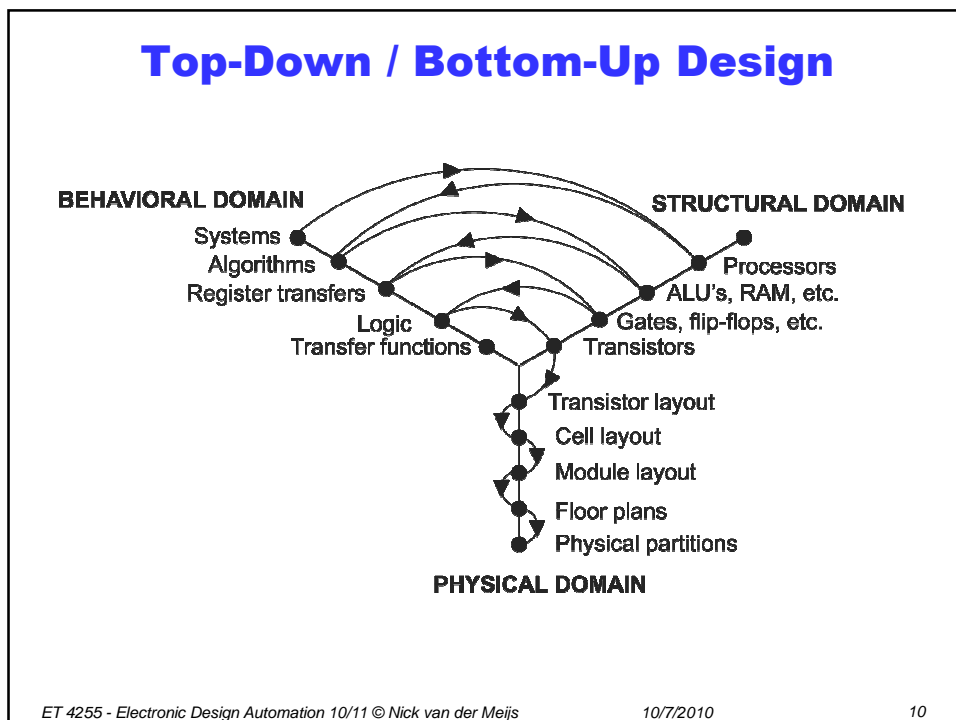
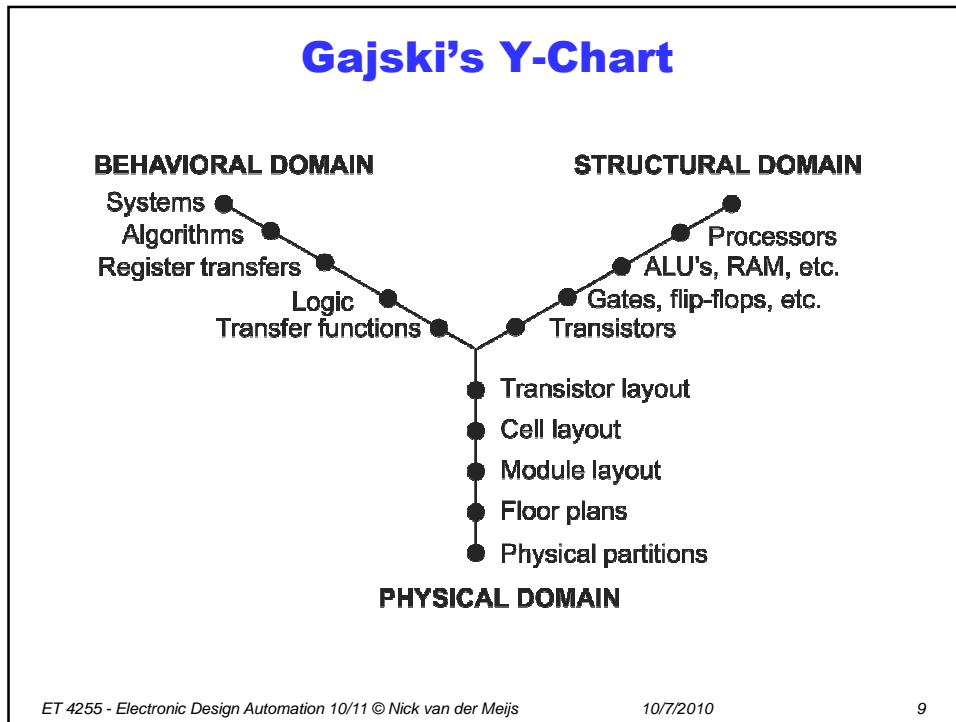
Design Domains

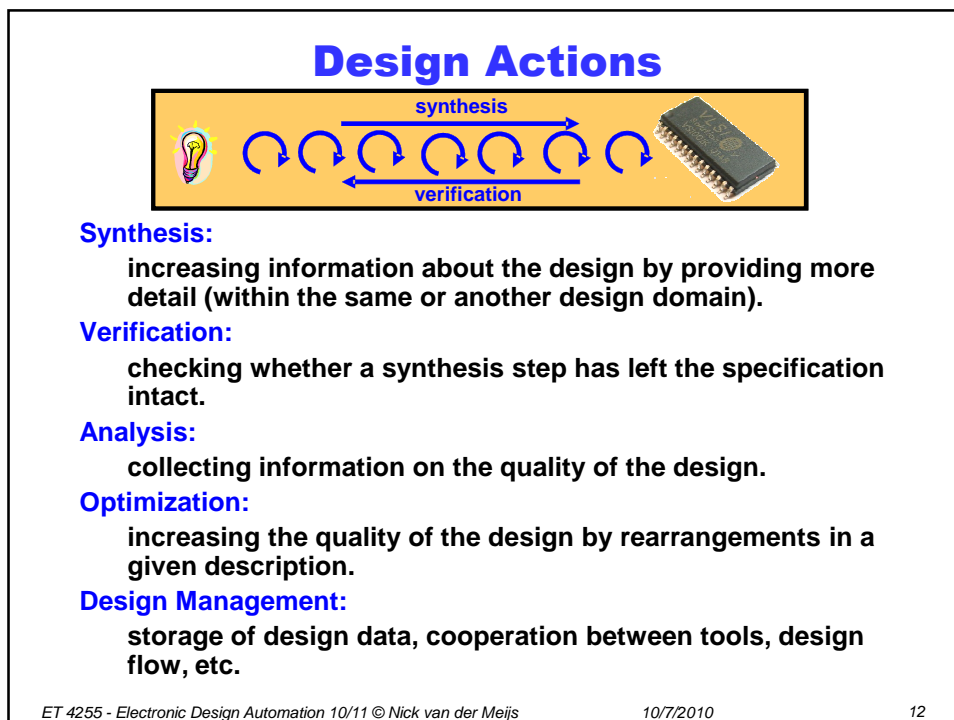
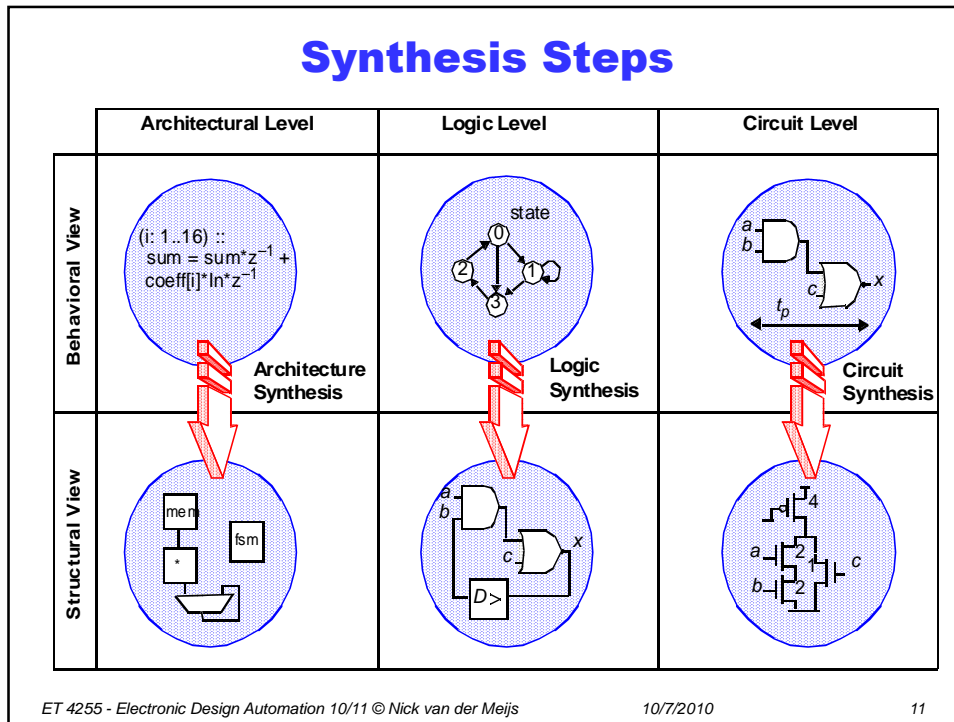
Design domains:

- **behavioral:** black box view
- **structural:** interconnection of subblocks
- **physical:** layout properties

Each design domain has its own hierarchy.

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Implementation Methods

Can the designer control the shape of all mask patterns?

Yes → full-custom fabrication

No → semi-custom fabrication, e.g. gate array, sea of gates

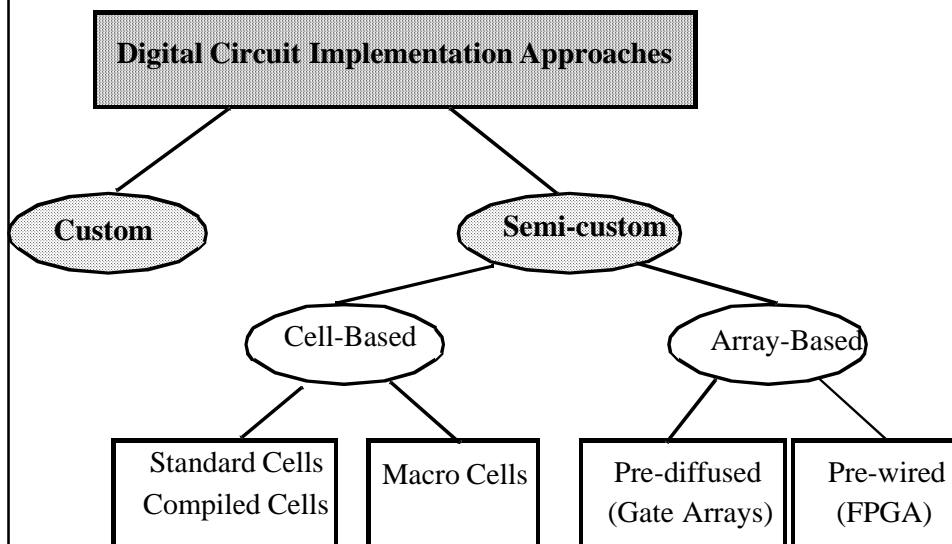
Can the designer specify the design up to the level of individual transistors?

Yes → full-custom design

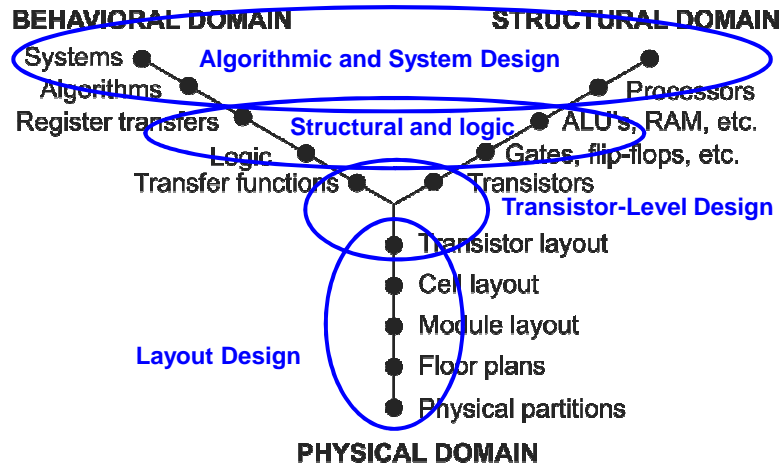
No → semi-custom design e.g. by means of standard cells, module generators, etc.

SPECIFIC DESIGN METHODS REQUIRE SPECIFIC CAD TOOLS!

Implementation Methods (2)



Coarse Classification



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Design Issues and Tools

System-level design:

- Partitioning into hardware and software, co-design, co-simulation, etc.
- Cost estimation, design-space exploration

Algorithmic-level design:

- Behavioral descriptions (e.g. in VHDL)
- High-level simulation

From algorithms to hardware modules:

- High-level (or architectural) synthesis

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Design Issues and Tools (2)

Logic design:

- Schematic entry
- Register-transfer level and logic synthesis
- Gate-level simulation (functionality, power)
- Timing analysis
- Formal verification

Transistor-level design:

- Switch-level simulation
- Circuit simulation

Design Issues and Tools (3)

Layout design:

- Floorplanning
- Module and cell generation
- Placement and routing
- Layout editing: symbolic and at mask level
- Layout compaction
- Design-rule checking
- Layout extraction

Design management:

- Data bases, frame works, etc.

Formal Verification

Computers are often used in safety-critical systems where a failure could cause loss of life.

- Health care: Heart pacemakers, radiation therapy machines
- Aircraft, Car engine management systems
- Nuclear reactor controllers
- Telephone exchanges (!)
- ...

Financial cost of bugs

- Even when not a matter of life and death, bugs can be financially serious if a faulty product has to be recalled or replaced. 1994 FDIV bug in the Intel Pentium processor

<http://www.emery.com/1e/pentium.htm>

http://en.wikipedia.org/wiki/Fdiv_bug

- Today, new products are ramped much faster...

Simulation can only prove presence of bugs, not absence!

Formal verification aims at **mathematically rigid proof of correctness of design**

More EDA Motivation

From **Microprocessor Watch**, Issue #7 MicroDesign Resources --- July 14, 1999

Intel Coppermine Hits Glitch

Intel's 0.18-micron Pentium III, code-named Coppermine, will be delayed until November. Sources indicate the problem is a speed path in the chip preventing operation above 550 MHz. The good news is that yields of the 0.25-micron Pentium III are strong enough to support a 600-MHz part in Q3, so PC buyers will see little impact from the delay. The Intel 820 (Camino) chip set remains scheduled for a September launch, enabling a 600/133 version at that time. We expect Coppermine to launch at 667 MHz in November.

The biggest impact will be on the mobile side, because the 0.25- micron Pentium III is too hot for notebook systems. Intel expects to ship Mobile Pentium III at speeds up to 500 MHz in September using the 0.18-micron process, but faster versions will be delayed. This delay will have a minimal impact on Intel's revenues: **\$100 million in Q4**, according to our estimates. Coupled with recent slips in Camino and Merced, however, the Coppermine delay shows that Intel's well-oiled development engine can occasionally sputter. --L.G.

Intel revenues (2003) : \$30.1 billion

<http://www.mdronline.com/publications/mpw/issues/mpw007.html>

Silicon Compilation holy grail of EDA

Analogy with compilers for programming languages:
algorithm → machine instructions

In VLSI:
algorithm → mask patterns

- **Current practice:**
- **This ideal is approached more and more (e.g. VHDL synthesis);**
- **Still far away from a single push-button operation.**
- **While old problems are solved, new problems appear because ongoing miniaturization exposes new physical effects**