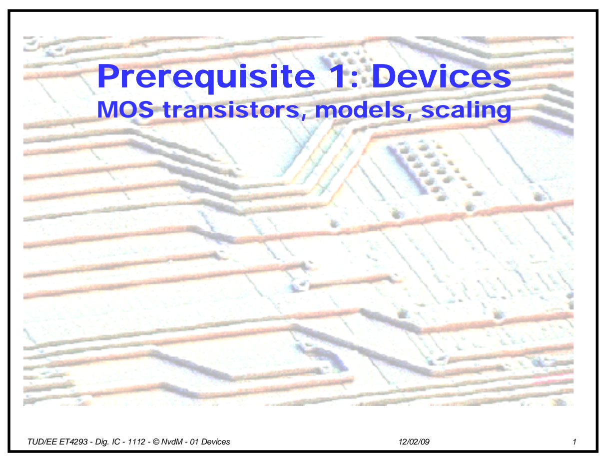
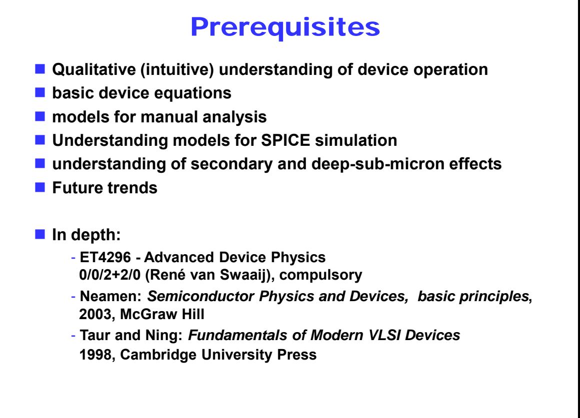
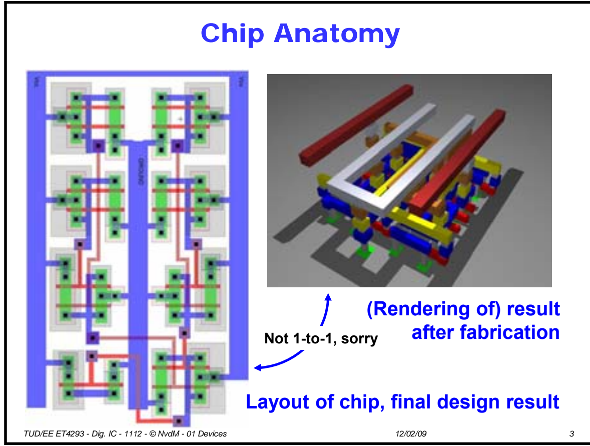
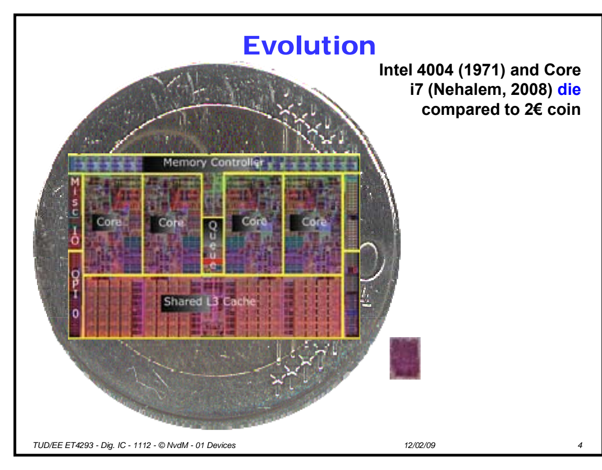
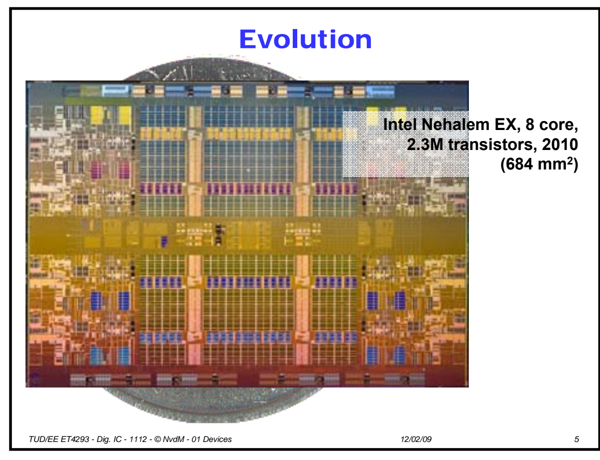
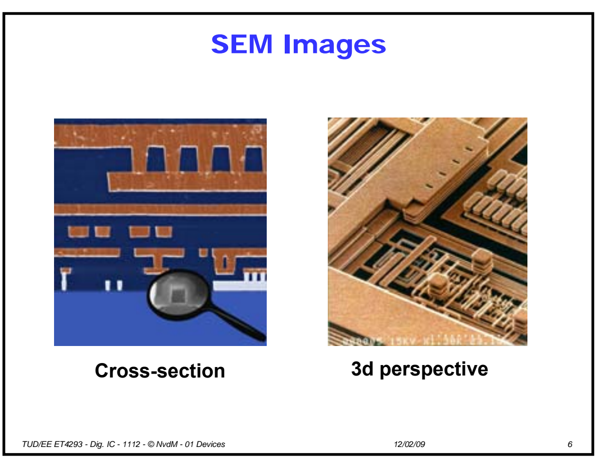

Prerequisite 1: Devices
MOS transistors, models, scaling
TUD/EE ET4293 - Dig. IC - 1112 - © NvdM - 01 Devices
12/02/09
1

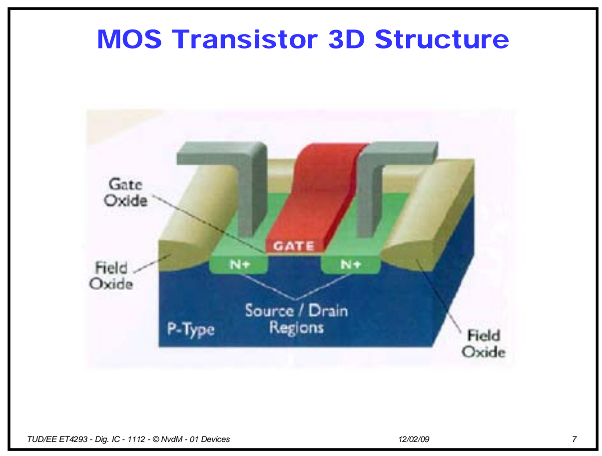

Prerequisites
Qualitative (intuitive) understanding of device operation
basic device equations
models for manual analysis
Understanding models for SPICE simulation
understanding of secondary and deep-sub-micron effects
Future trends
In depth:
- ET4296 - Advanced Device Physics
0/0/2+2/0 (René van Swaaij), compulsory
- Neamen: Semiconductor Physics and Devices, basic principles, 2003, McGraw Hill
- Taur and Ning: Fundamentals of Modern VLSI Devices
1998, Cambridge University Press
TUD/EE ET4293 - Dig. IC - 1112 - © NvdM - 01 Devices
12/02/09
2

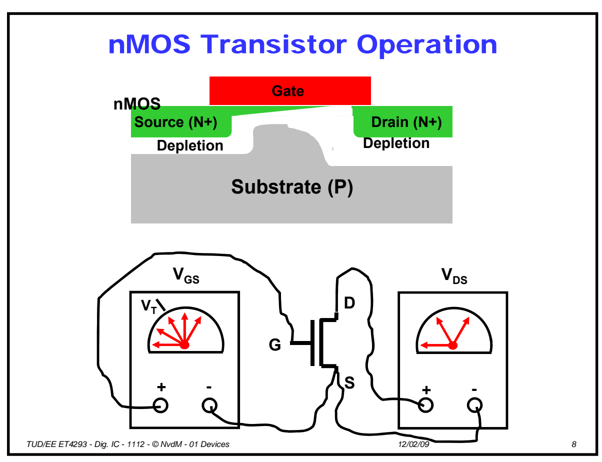

Chip Anatomy
(Rendering of) result
after fabrication
Not 1-to-1, sorry
Layout of chip, final design result
TUD/EE ET4293 - Dig. IC - 1112 - © NvdM - 01 Devices
12/02/09
3

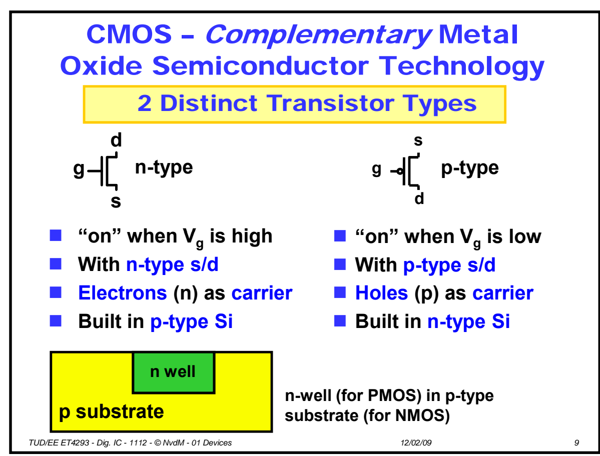

Evolution
Intel 4004 (1971) and Core i7 (Nehalem, 2008) die compared to 2€ coin
Memory Controller
Core
Core
Core
Core
Queue
Shared L3 Cache
TUD/EE ET4293 - Dig. IC - 1112 - © NvdM - 01 Devices
12/02/09
4

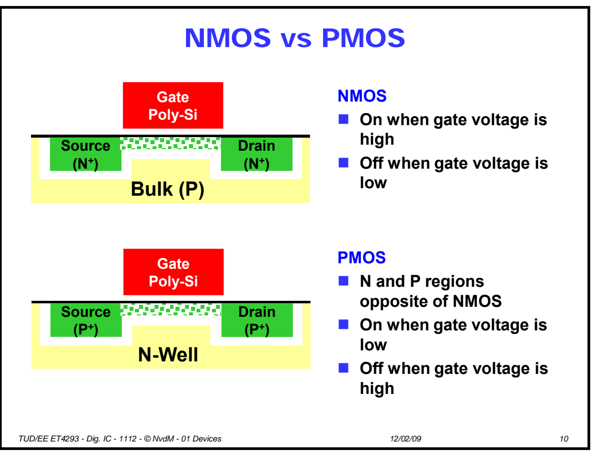

Evolution
Intel Nehalem EX, 8 core,
2.3M transistors, 2010
(684 mm²)
TUD/EE ET4293 - Dig. IC - 1112 - © NvdM - 01 Devices
12/02/09
5

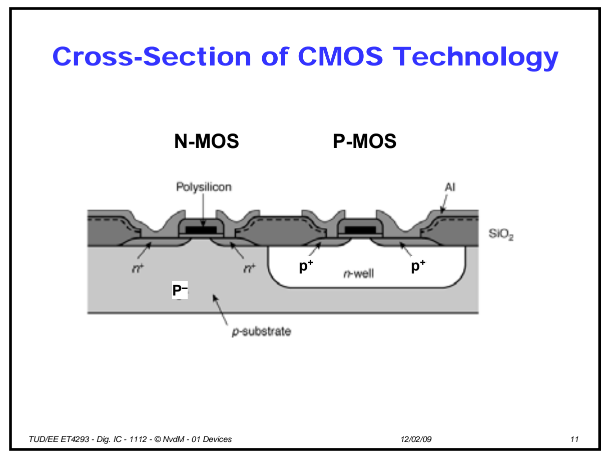

SEM Images
Cross-section
3d perspective
TUD/EE ET4293 - Dig. IC - 1112 - © NvdM - 01 Devices
12/02/09
6

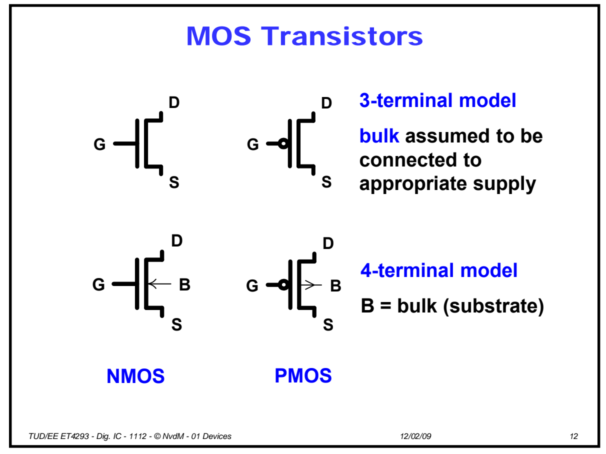

MOS Transistor 3D Structure
Gate Oxide
Field Oxide
GATE
N+
N+
Source / Drain Regions
P-Type
Field Oxide
TUD/EE ET4293 - Dig. IC - 1112 - © NvdM - 01 Devices
12/02/09
7

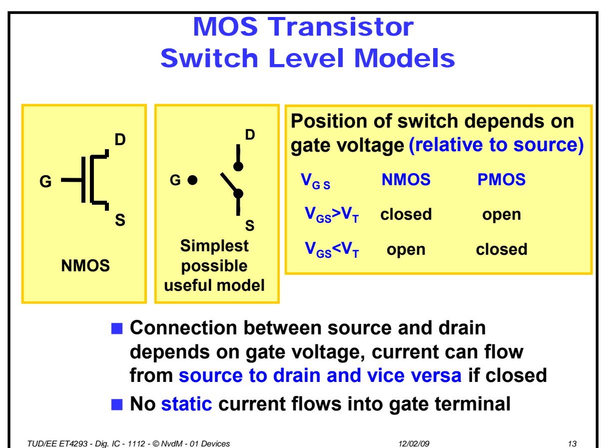

nMOS Transistor Operation
Gate
nMOS
Source (N+)
Drain (N+)
Depletion
Depletion
Substrate (P)
V_{GS}
V_{DS}
V_T
D
G
S
TUD/EE ET4293 - Dig. IC - 1112 - © NvdM - 01 Devices
12/02/09
8

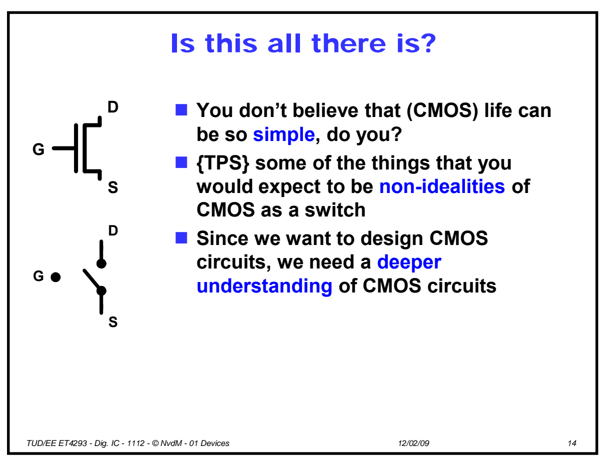

CMOS – Complementary Metal Oxide Semiconductor Technology
2 Distinct Transistor Types
n-type
p-type
"on" when V_g is high
With n-type s/d
Electrons (n) as carrier
Built in p-type Si
"on" when V_g is low
With p-type s/d
Holes (p) as carrier
Built in n-type Si
n well
p substrate
n-well (for PMOS) in p-type substrate (for NMOS)
TUD/EE ET4293 - Dig. IC - 1112 - © NvdM - 01 Devices
12/02/09
9

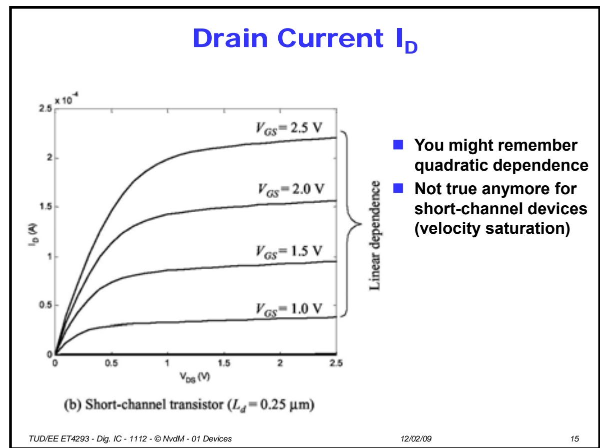

NMOS vs PMOS
Gate Poly-Si
Source (N+)
Drain (N+)
Bulk (P)
NMOS
On when gate voltage is high
Off when gate voltage is low
Gate Poly-Si
Source (P+)
Drain (P+)
N-Well
PMOS
N and P regions opposite of NMOS
On when gate voltage is low
Off when gate voltage is high
TUD/EE ET4293 - Dig. IC - 1112 - © NvdM - 01 Devices
12/02/09
10

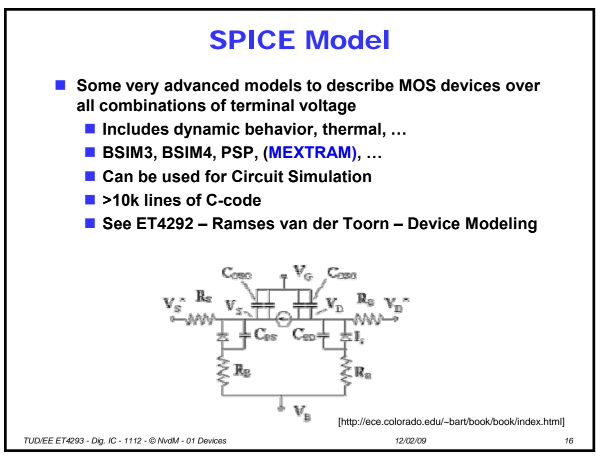

Cross-Section of CMOS Technology
N-MOS
P-MOS
Polysilicon
Al
SiO_2
n^+
n^+
p^+
n-well
p^+
p-substrate
TUD/EE ET4293 - Dig. IC - 1112 - © NvdM - 01 Devices
12/02/09
11

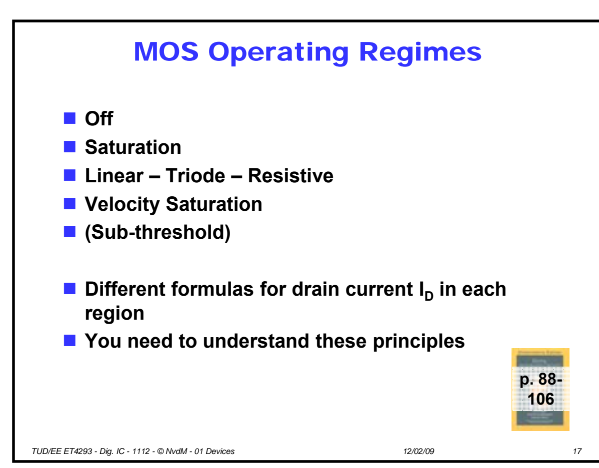

MOS Transistors
3-terminal model
bulk assumed to be connected to appropriate supply
4-terminal model
B = bulk (substrate)
NMOS
PMOS
TUD/EE ET4293 - Dig. IC - 1112 - © NvdM - 01 Devices
12/02/09
12

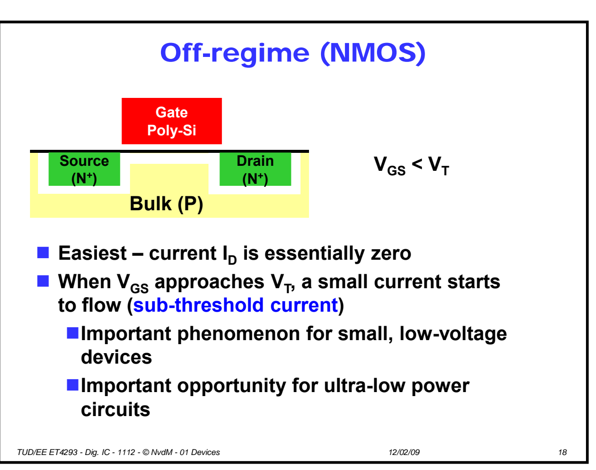

MOS Transistor
Switch Level Models
D
G
S
NMOS
D
G
S
Simplest possible useful model
Position of switch depends on gate voltage (relative to source)
VGS NMOS PMOS
VGS>VT closed open
VGS<VT open closed
Connection between source and drain depends on gate voltage, current can flow from source to drain and vice versa if closed
No static current flows into gate terminal
TUD/EE ET4293 - Dig. IC - 1112 - © NvdM - 01 Devices 12/02/09 13

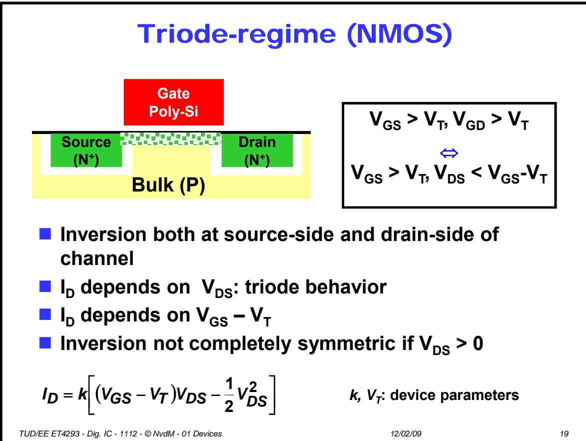

Is this all there is?
You don't believe that (CMOS) life can be so simple, do you?
{TPS} some of the things that you would expect to be non-idealities of CMOS as a switch
Since we want to design CMOS circuits, we need a deeper understanding of CMOS circuits
TUD/EE ET4293 - Dig. IC - 1112 - © NvdM - 01 Devices 12/02/09 14

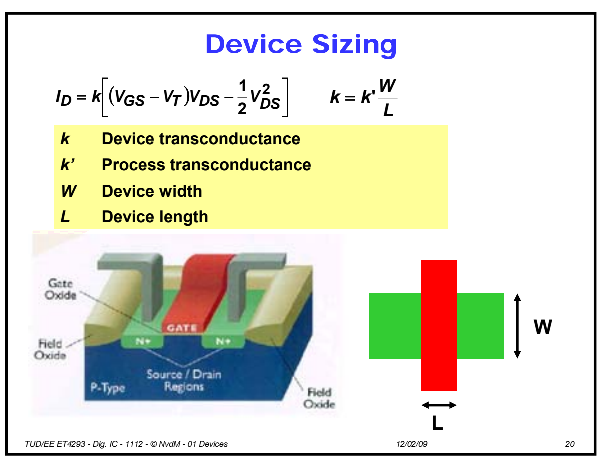

Drain Current ID
VGS= 2.5 V
VGS= 2.0 V
VGS= 1.5 V
VGS= 1.0 V
Linear dependence
VDS (V)
(b) Short-channel transistor (Ld = 0.25 µm)
You might remember quadratic dependence
Not true anymore for short-channel devices (velocity saturation)
TUD/EE ET4293 - Dig. IC - 1112 - © NvdM - 01 Devices 12/02/09 15

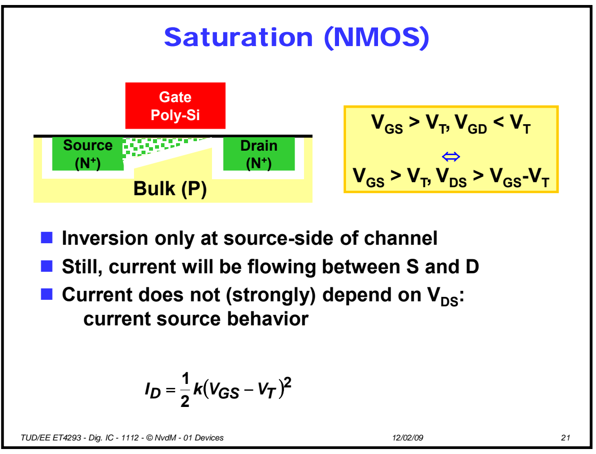

SPICE Model
Some very advanced models to describe MOS devices over all combinations of terminal voltage
Includes dynamic behavior, thermal, …
BSIM3, BSIM4, PSP, (MEXTRAM), …
Can be used for Circuit Simulation
>10k lines of C-code
See ET4292 – Ramses van der Toorn – Device Modeling
[http://ece.colorado.edu/~bart/book/book/index.html]
TUD/EE ET4293 - Dig. IC - 1112 - © NvdM - 01 Devices 12/02/09 16

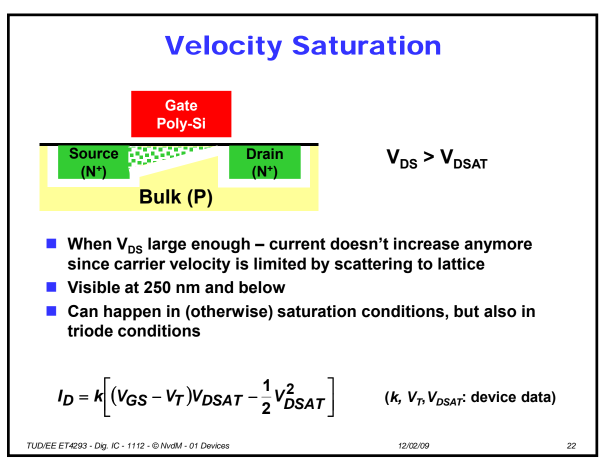

MOS Operating Regimes
Off
Saturation
Linear – Triode – Resistive
Velocity Saturation
(Sub-threshold)
Different formulas for drain current ID in each region
You need to understand these principles
p. 88-106
TUD/EE ET4293 - Dig. IC - 1112 - © NvdM - 01 Devices 12/02/09 17

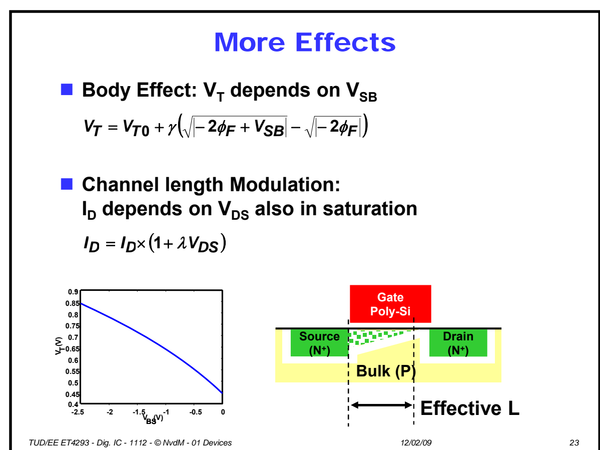

Off-regime (NMOS)
Gate Poly-Si
Source (N+)
Drain (N+)
Bulk (P)
VGS < VT
Easiest – current ID is essentially zero
When VGS approaches VT, a small current starts to flow (sub-threshold current)
Important phenomenon for small, low-voltage devices
Important opportunity for ultra-low power circuits
TUD/EE ET4293 - Dig. IC - 1112 - © NvdM - 01 Devices 12/02/09 18

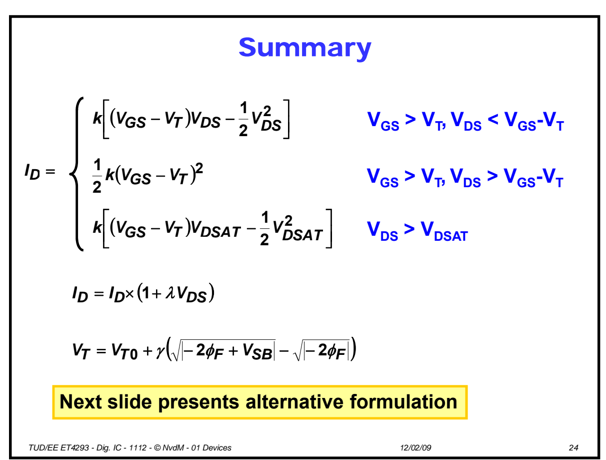

Triode-regime (NMOS)
Gate Poly-Si
Source (N+)
Drain (N+)
Bulk (P)
$V_{GS} > V_T, V_{GD} > V_T$
⇔
$V_{GS} > V_T, V_{DS} < V_{GS}-V_T$
Inversion both at source-side and drain-side of channel
I_D depends on V_{DS}: triode behavior
I_D depends on $V_{GS} - V_T$
Inversion not completely symmetric if $V_{DS} > 0$
$I_D = k\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right]$
k, V_T: device parameters
TUD/EE ET4293 - Dig. IC - 1112 - © NvdM - 01 Devices
12/02/09
19

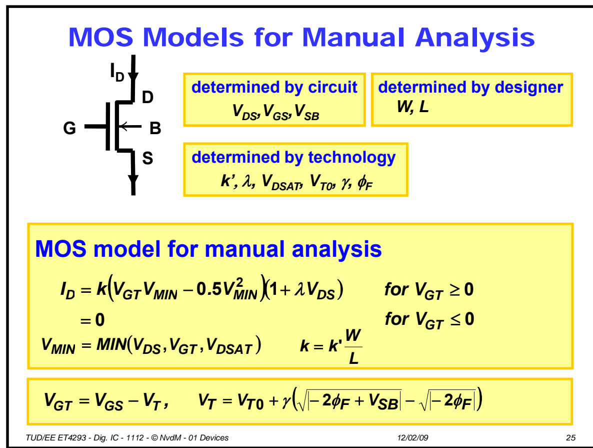

Device Sizing
$I_D = k\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right]$
$k = k'\frac{W}{L}$
k Device transconductance
k' Process transconductance
W Device width
L Device length
Gate Oxide
Field Oxide
GATE
N+
N+
Source / Drain Regions
P-Type
Field Oxide
W
L
TUD/EE ET4293 - Dig. IC - 1112 - © NvdM - 01 Devices
12/02/09
20

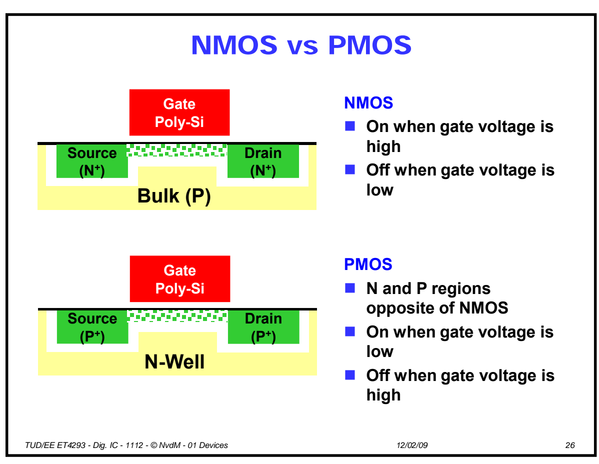

Saturation (NMOS)
Gate Poly-Si
Source (N+)
Drain (N+)
Bulk (P)
$V_{GS} > V_T, V_{GD} < V_T$
⇔
$V_{GS} > V_T, V_{DS} > V_{GS}-V_T$
Inversion only at source-side of channel
Still, current will be flowing between S and D
Current does not (strongly) depend on V_{DS}: current source behavior
$I_D = \frac{1}{2}k(V_{GS} - V_T)^2$
TUD/EE ET4293 - Dig. IC - 1112 - © NvdM - 01 Devices
12/02/09
21

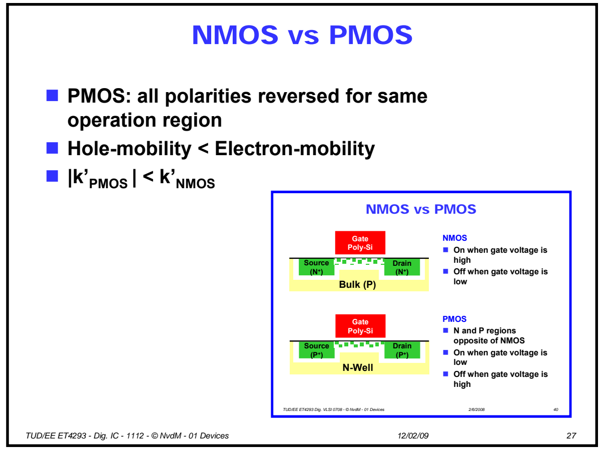

Velocity Saturation
Gate Poly-Si
Source (N+)
Drain (N+)
Bulk (P)
$V_{DS} > V_{DSAT}$
When V_{DS} large enough – current doesn't increase anymore since carrier velocity is limited by scattering to lattice
Visible at 250 nm and below
Can happen in (otherwise) saturation conditions, but also in triode conditions
$I_D = k\left[(V_{GS} - V_T)V_{DSAT} - \frac{1}{2}V_{DSAT}^2\right]$
(k, V_T, V_{DSAT}: device data)
TUD/EE ET4293 - Dig. IC - 1112 - © NvdM - 01 Devices
12/02/09
22

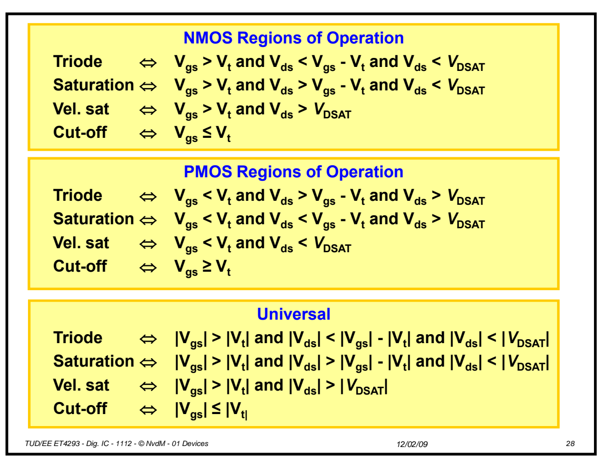

More Effects
Body Effect: V_T depends on V_{SB}
$V_T = V_{T0} + \gamma\left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|}\right)$
Channel length Modulation:
I_D depends on V_{DS} also in saturation
$I_D = I_D \times (1 + \lambda V_{DS})$
V_T (V)
V_{BS} (V)
Gate Poly-Si
Source (N+)
Drain (N+)
Bulk (P)
Effective L
TUD/EE ET4293 - Dig. IC - 1112 - © NvdM - 01 Devices
12/02/09
23

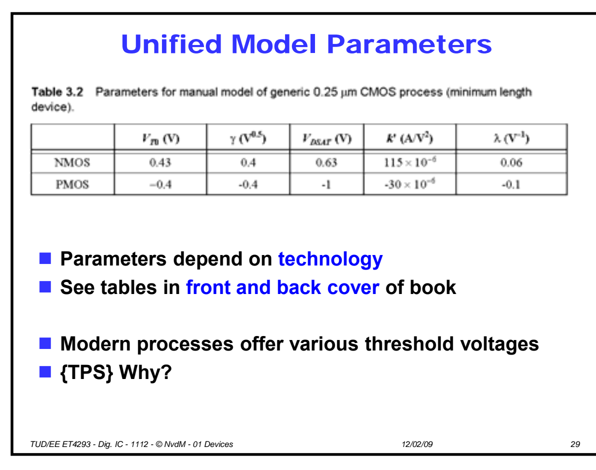

Summary
$I_D = \begin{cases} k\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right] & V_{GS} > V_T, V_{DS} < V_{GS}-V_T \\ \frac{1}{2}k(V_{GS} - V_T)^2 & V_{GS} > V_T, V_{DS} > V_{GS}-V_T \\ k\left[(V_{GS} - V_T)V_{DSAT} - \frac{1}{2}V_{DSAT}^2\right] & V_{DS} > V_{DSAT} \end{cases}$
$I_D = I_D \times (1 + \lambda V_{DS})$
$V_T = V_{T0} + \gamma\left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|}\right)$
Next slide presents alternative formulation
TUD/EE ET4293 - Dig. IC - 1112 - © NvdM - 01 Devices
12/02/09
24







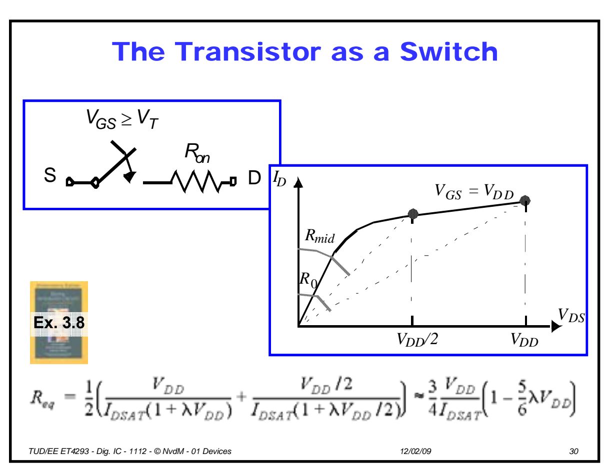


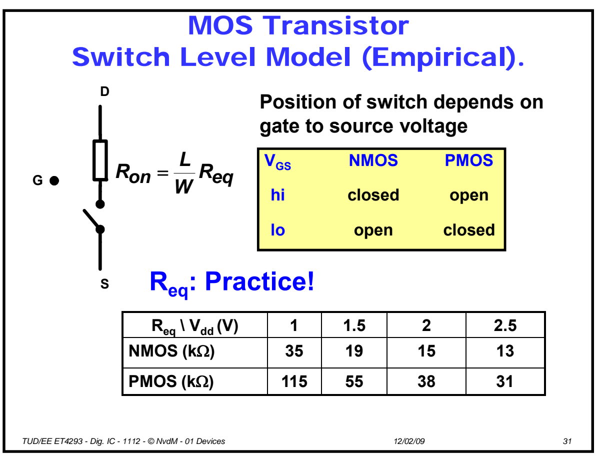


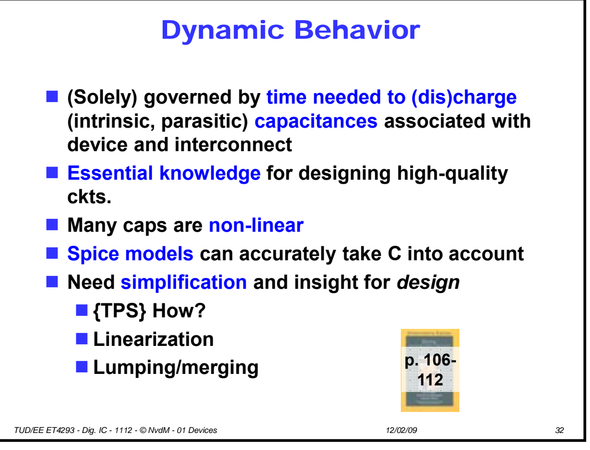
Unified Model Parameters

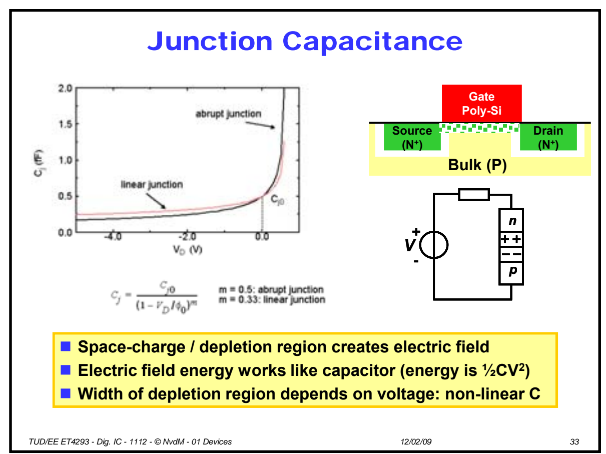
Table 3.2 Parameters for manual model of generic 0.25 μm CMOS process (minimum length device).

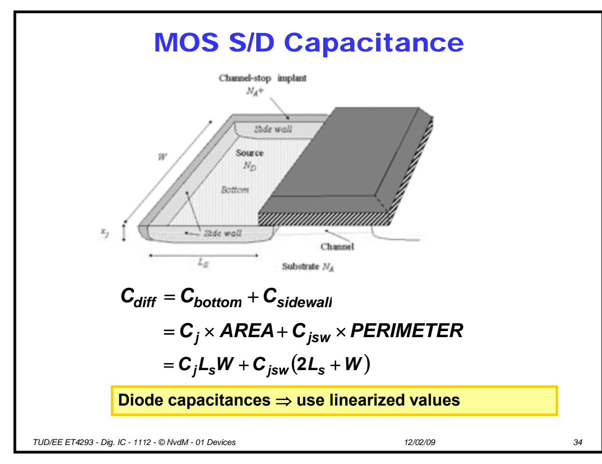
	V_{T0} (V)	γ ($V^{0.5}$)	V_{DSAT} (V)	k' (A/V²)	λ (V^{-1})
NMOS	0.43	0.4	0.63	115×10^{-6}	0.06
PMOS	−0.4	-0.4	-1	-30×10^{-6}	-0.1

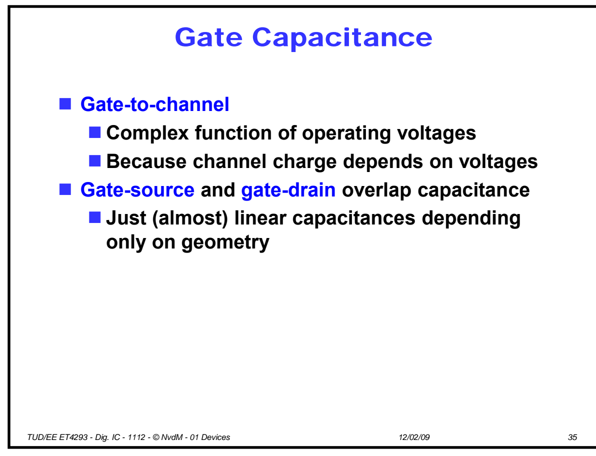


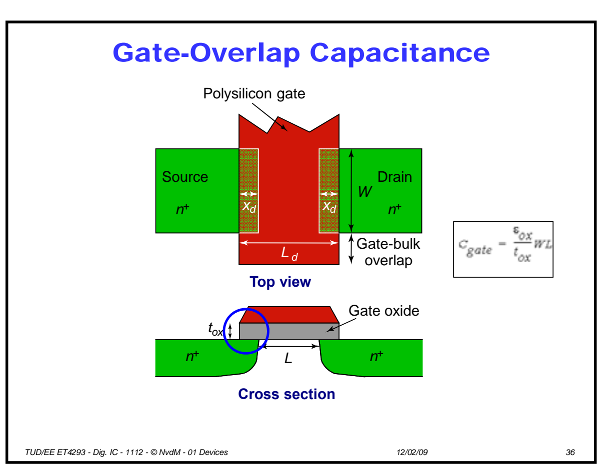

MOS Transistor
Switch Level Model (Empirical).
D
G
S
$R_{on} = \frac{L}{W} R_{eq}$
Position of switch depends on gate to source voltage
VGS NMOS PMOS
hi closed open
lo open closed
Req: Practice!
Req \ Vdd (V) 1 1.5 2 2.5
NMOS (kΩ) 35 19 15 13
PMOS (kΩ) 115 55 38 31
TUD/EE ET4293 - Dig. IC - 1112 - © NvdM - 01 Devices 12/02/09 31

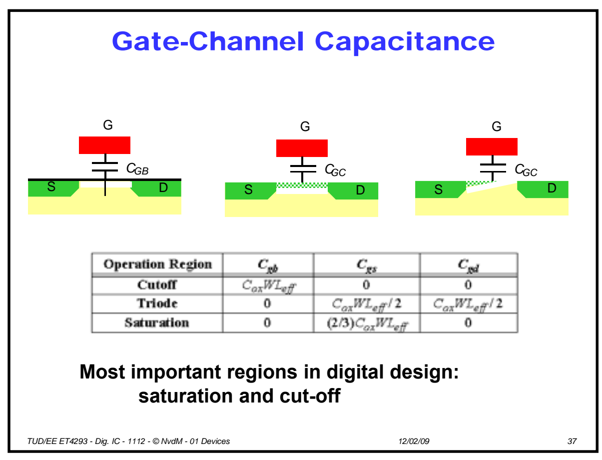

Dynamic Behavior
(Solely) governed by time needed to (dis)charge (intrinsic, parasitic) capacitances associated with device and interconnect
Essential knowledge for designing high-quality ckts.
Many caps are non-linear
Spice models can accurately take C into account
Need simplification and insight for design
{TPS} How?
Linearization
Lumping/merging
p. 106-112
TUD/EE ET4293 - Dig. IC - 1112 - © NvdM - 01 Devices 12/02/09 32

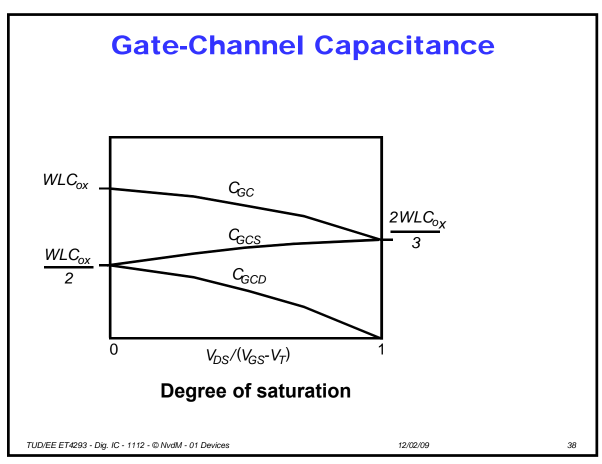

Junction Capacitance
abrupt junction
linear junction
Gate Poly-Si
Source (N+)
Drain (N+)
Bulk (P)
m = 0.5: abrupt junction
m = 0.33: linear junction
Space-charge / depletion region creates electric field
Electric field energy works like capacitor (energy is ½CV²)
Width of depletion region depends on voltage: non-linear C
TUD/EE ET4293 - Dig. IC - 1112 - © NvdM - 01 Devices 12/02/09 33

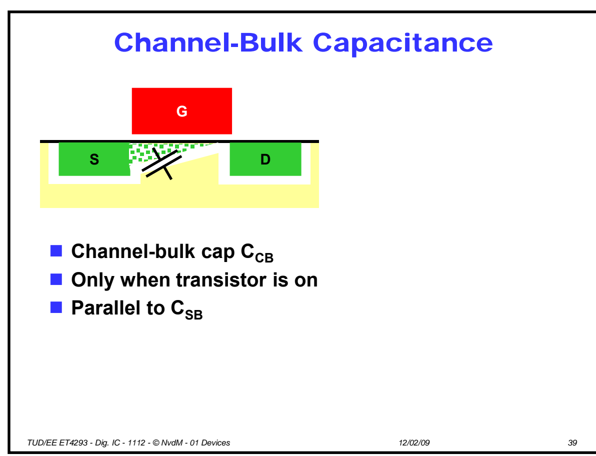

MOS S/D Capacitance
Channel-stop implant
Side wall
Source
Bottom
Channel
Substrate
$C_{diff} = C_{bottom} + C_{sidewall}$
$= C_j \times AREA + C_{jsw} \times PERIMETER$
$= C_j L_s W + C_{jsw}(2L_s + W)$
Diode capacitances ⇒ use linearized values
TUD/EE ET4293 - Dig. IC - 1112 - © NvdM - 01 Devices 12/02/09 34

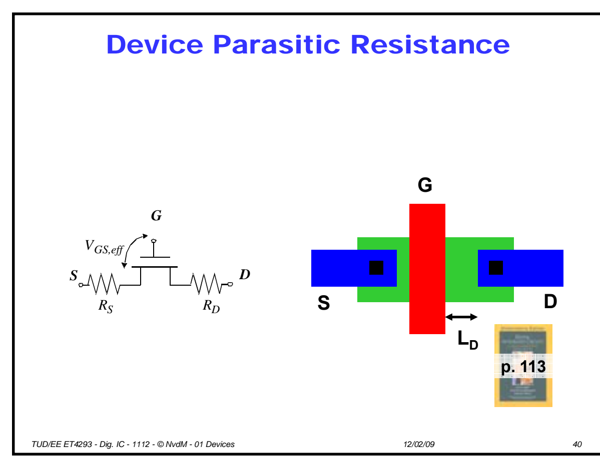

Gate Capacitance
Gate-to-channel
Complex function of operating voltages
Because channel charge depends on voltages
Gate-source and gate-drain overlap capacitance
Just (almost) linear capacitances depending only on geometry
TUD/EE ET4293 - Dig. IC - 1112 - © NvdM - 01 Devices 12/02/09 35

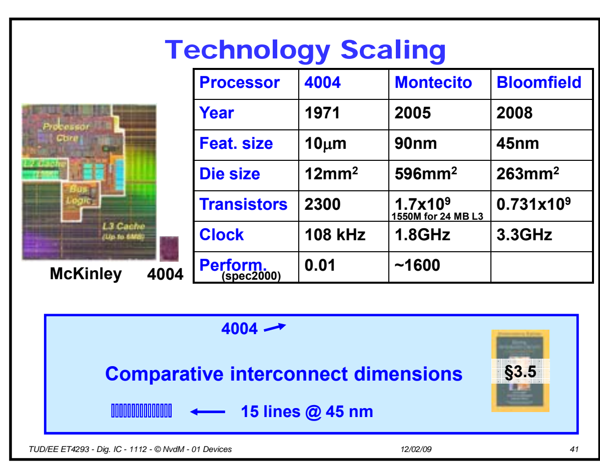

Gate-Overlap Capacitance
Polysilicon gate
Source
Drain
Gate-bulk overlap
Top view
Gate oxide
Cross section
TUD/EE ET4293 - Dig. IC - 1112 - © NvdM - 01 Devices 12/02/09 36

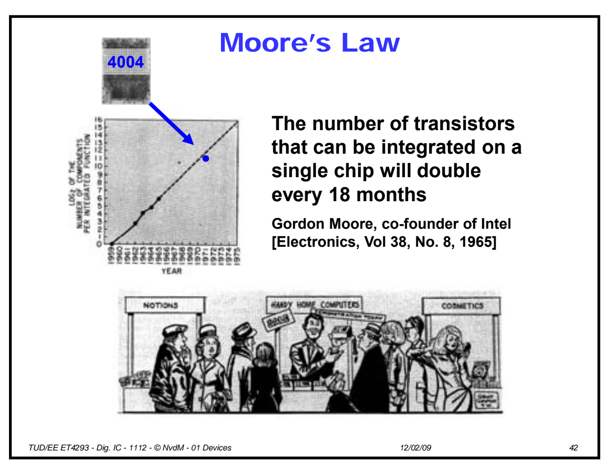

Gate-Channel Capacitance
G
C_{GB}
S
D
G
C_{GC}
G
C_{GC}
Operation Region | C_{gb} | C_{gs} | C_{gd}
Cutoff | $C_{ox}WL_{eff}$ | 0 | 0
Triode | 0 | $C_{ox}WL_{eff}/2$ | $C_{ox}WL_{eff}/2$
Saturation | 0 | $(2/3)C_{ox}WL_{eff}$ | 0
Most important regions in digital design:
saturation and cut-off
TUD/EE ET4293 - Dig. IC - 1112 - © NvdM - 01 Devices
12/02/09
37

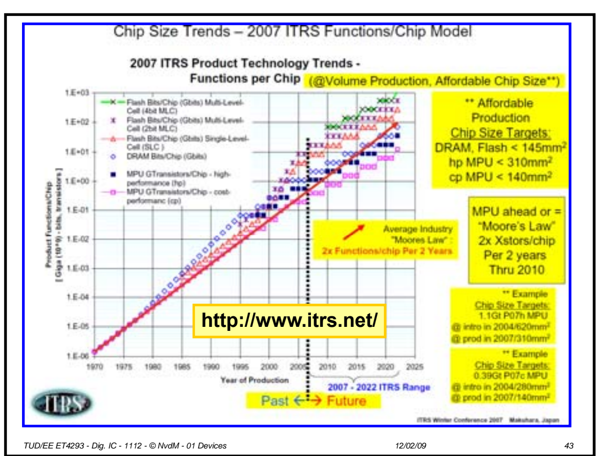

Gate-Channel Capacitance
WLC_{ox}
C_{GC}
$\frac{2WLC_{ox}}{3}$
C_{GCS}
$\frac{WLC_{ox}}{2}$
C_{GCD}
0
$V_{DS}/(V_{GS}-V_T)$
1
Degree of saturation
TUD/EE ET4293 - Dig. IC - 1112 - © NvdM - 01 Devices
12/02/09
38

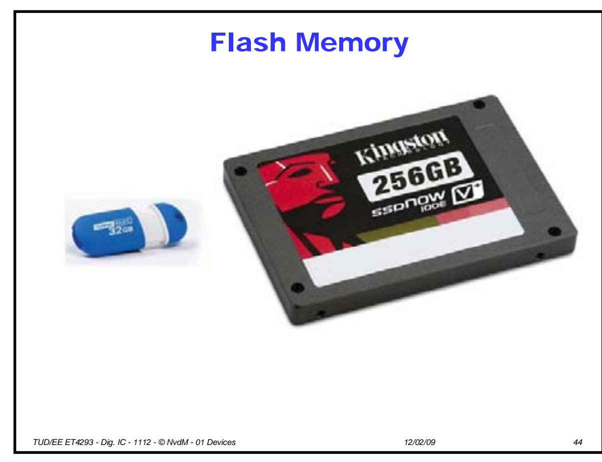

Channel-Bulk Capacitance
G
S
D
Channel-bulk cap C_{CB}
Only when transistor is on
Parallel to C_{SB}
TUD/EE ET4293 - Dig. IC - 1112 - © NvdM - 01 Devices
12/02/09
39

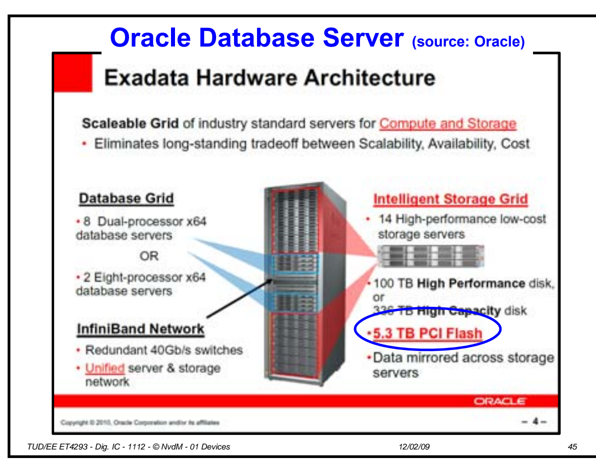

Device Parasitic Resistance
G
$V_{GS,eff}$
S
D
R_S
R_D
G
S
D
L_D
p. 113
TUD/EE ET4293 - Dig. IC - 1112 - © NvdM - 01 Devices
12/02/09
40


Technology Scaling
Processor | 4004 | Montecito | Bloomfield
Year | 1971 | 2005 | 2008
Feat. size | 10µm | 90nm | 45nm
Die size | 12mm² | 596mm² | 263mm²
Transistors | 2300 | 1.7x10⁹ 1550M for 24 MB L3 | 0.731x10⁹
Clock | 108 kHz | 1.8GHz | 3.3GHz
Perform. (spec2000) | 0.01 | ~1600 |
Processor Core
Bus Logic
L3 Cache
McKinley
4004
4004
Comparative interconnect dimensions
§3.5
15 lines @ 45 nm
TUD/EE ET4293 - Dig. IC - 1112 - © NvdM - 01 Devices
12/02/09
41


Moore's Law
4004
The number of transistors that can be integrated on a single chip will double every 18 months
Gordon Moore, co-founder of Intel [Electronics, Vol 38, No. 8, 1965]
YEAR
NOTIONS
HANDY HOME COMPUTERS
COSMETICS
TUD/EE ET4293 - Dig. IC - 1112 - © NvdM - 01 Devices
12/02/09
42


Chip Size Trends – 2007 ITRS Functions/Chip Model
2007 ITRS Product Technology Trends - Functions per Chip
(@Volume Production, Affordable Chip Size**)
** Affordable Production Chip Size Targets: DRAM, Flash < 145mm²; hp MPU < 310mm²; cp MPU < 140mm²
MPU ahead or = "Moore's Law" 2x Xstors/chip Per 2 years Thru 2010
Average Industry "Moores Law": 2x Functions/chip Per 2 Years
http://www.itrs.net/
Year of Production
2007 - 2022 ITRS Range
Past ← → Future
TUD/EE ET4293 - Dig. IC - 1112 - © NvdM - 01 Devices
12/02/09
43


Flash Memory
Kingston
256GB
SSDNOW V
TUD/EE ET4293 - Dig. IC - 1112 - © NvdM - 01 Devices
12/02/09
44


Oracle Database Server (source: Oracle)
Exadata Hardware Architecture
Scaleable Grid of industry standard servers for Compute and Storage
• Eliminates long-standing tradeoff between Scalability, Availability, Cost
Database Grid
• 8 Dual-processor x64 database servers
OR
• 2 Eight-processor x64 database servers
InfiniBand Network
• Redundant 40Gb/s switches
• Unified server & storage network
Intelligent Storage Grid
• 14 High-performance low-cost storage servers
• 100 TB High Performance disk, or
336 TB High Capacity disk
• 5.3 TB PCI Flash
• Data mirrored across storage servers
ORACLE
TUD/EE ET4293 - Dig. IC - 1112 - © NvdM - 01 Devices
12/02/09
45

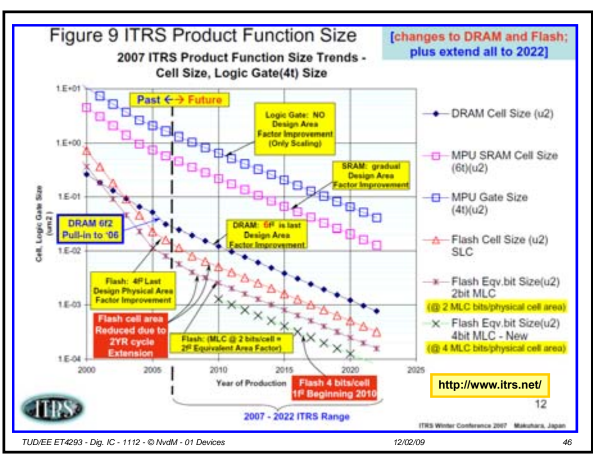
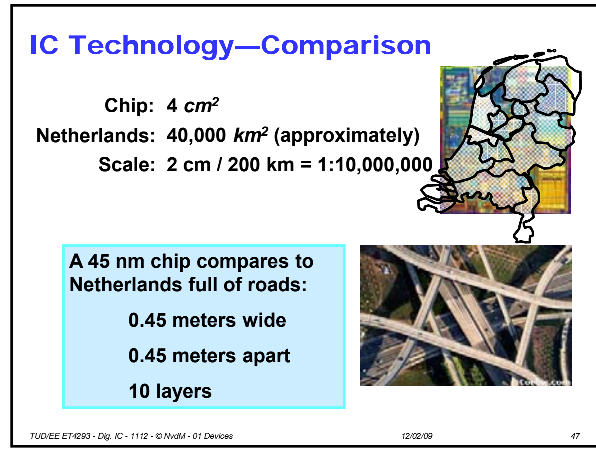
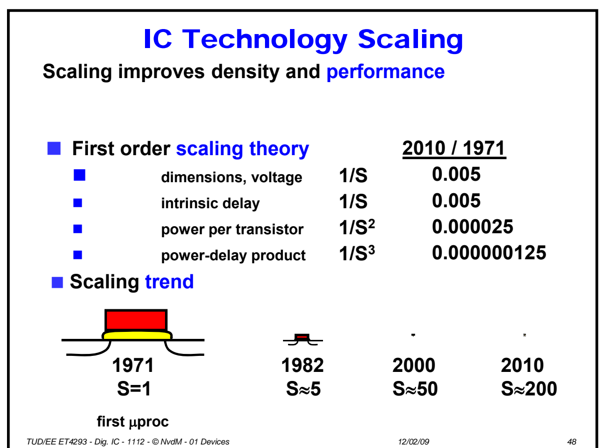
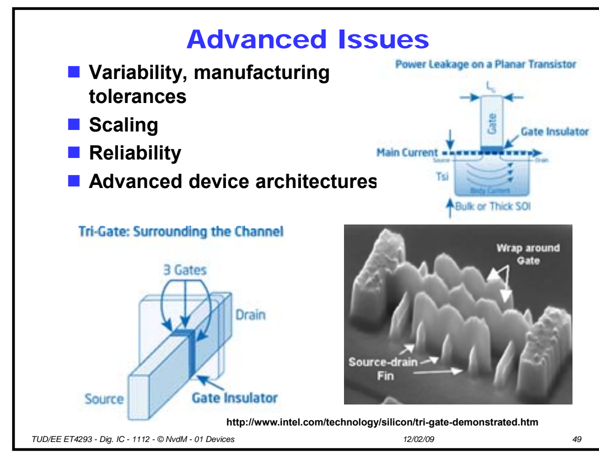
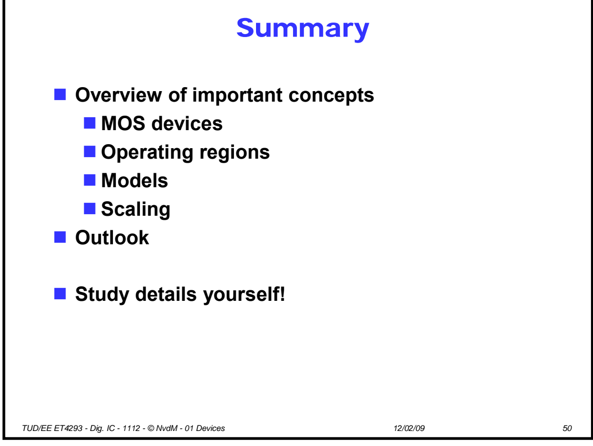


Figure 9 ITRS Product Function Size
[changes to DRAM and Flash; plus extend all to 2022]
2007 ITRS Product Function Size Trends - Cell Size, Logic Gate(4t) Size
Past ← → Future
DRAM Cell Size (u2)
MPU SRAM Cell Size (6t)(u2)
MPU Gate Size (4t)(u2)
Flash Cell Size (u2) SLC
Flash Eqv.bit Size(u2) 2bit MLC
Flash Eqv.bit Size(u2) 4bit MLC - New
Year of Production
Flash 4 bits/cell 1st Beginning 2010
http://www.itrs.net/
2007 - 2022 ITRS Range
TUD/EE ET4293 - Dig. IC - 1112 - © NvdM - 01 Devices
12/02/09
46


IC Technology—Comparison
Chip: 4 cm²
Netherlands: 40,000 km² (approximately)
Scale: 2 cm / 200 km = 1:10,000,000
A 45 nm chip compares to Netherlands full of roads:
0.45 meters wide
0.45 meters apart
10 layers
TUD/EE ET4293 - Dig. IC - 1112 - © NvdM - 01 Devices
12/02/09
47


IC Technology Scaling
Scaling improves density and performance
First order scaling theory
2010 / 1971
dimensions, voltage 1/S 0.005
intrinsic delay 1/S 0.005
power per transistor 1/S² 0.000025
power-delay product 1/S³ 0.000000125
Scaling trend
1971 S=1
1982 S≈5
2000 S≈50
2010 S≈200
first μproc
TUD/EE ET4293 - Dig. IC - 1112 - © NvdM - 01 Devices
12/02/09
48


Advanced Issues
Variability, manufacturing tolerances
Scaling
Reliability
Advanced device architectures
Power Leakage on a Planar Transistor
Gate
Gate Insulator
Main Current
Tsi
Bulk or Thick SOI
Tri-Gate: Surrounding the Channel
3 Gates
Drain
Source
Gate Insulator
Wrap around Gate
Source-drain Fin
http://www.intel.com/technology/silicon/tri-gate-demonstrated.htm
TUD/EE ET4293 - Dig. IC - 1112 - © NvdM - 01 Devices
12/02/09
49


Summary
Overview of important concepts
MOS devices
Operating regions
Models
Scaling
Outlook
Study details yourself!
TUD/EE ET4293 - Dig. IC - 1112 - © NvdM - 01 Devices
12/02/09
50