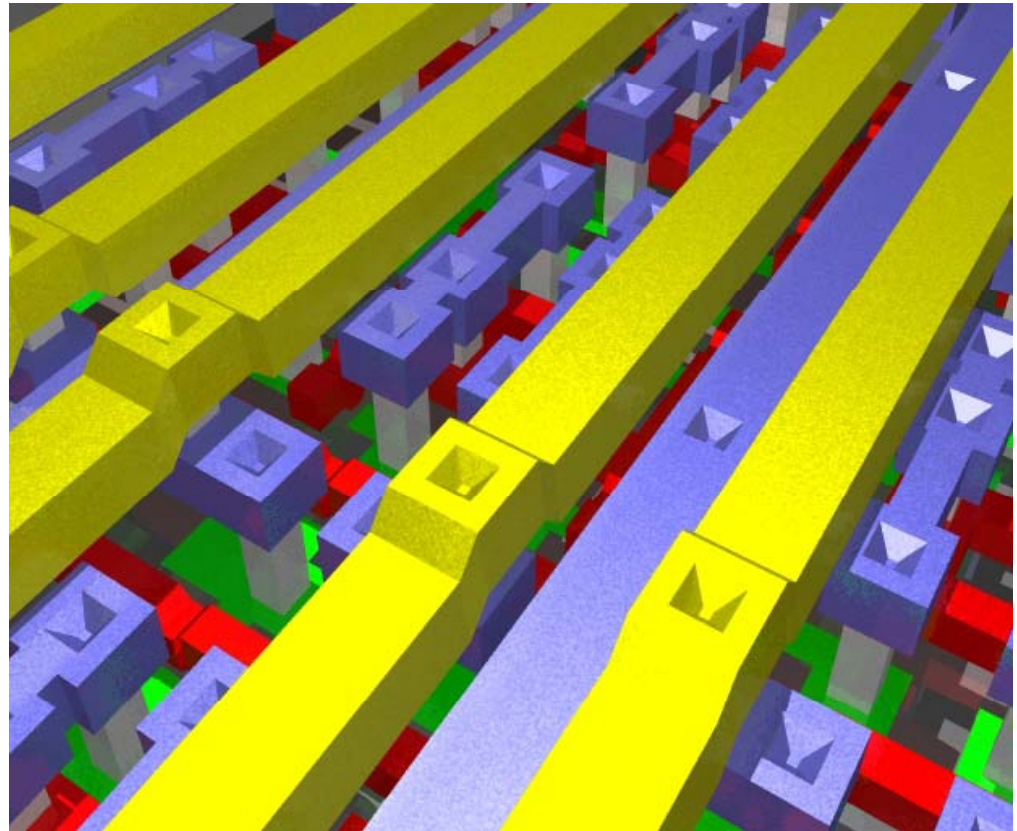


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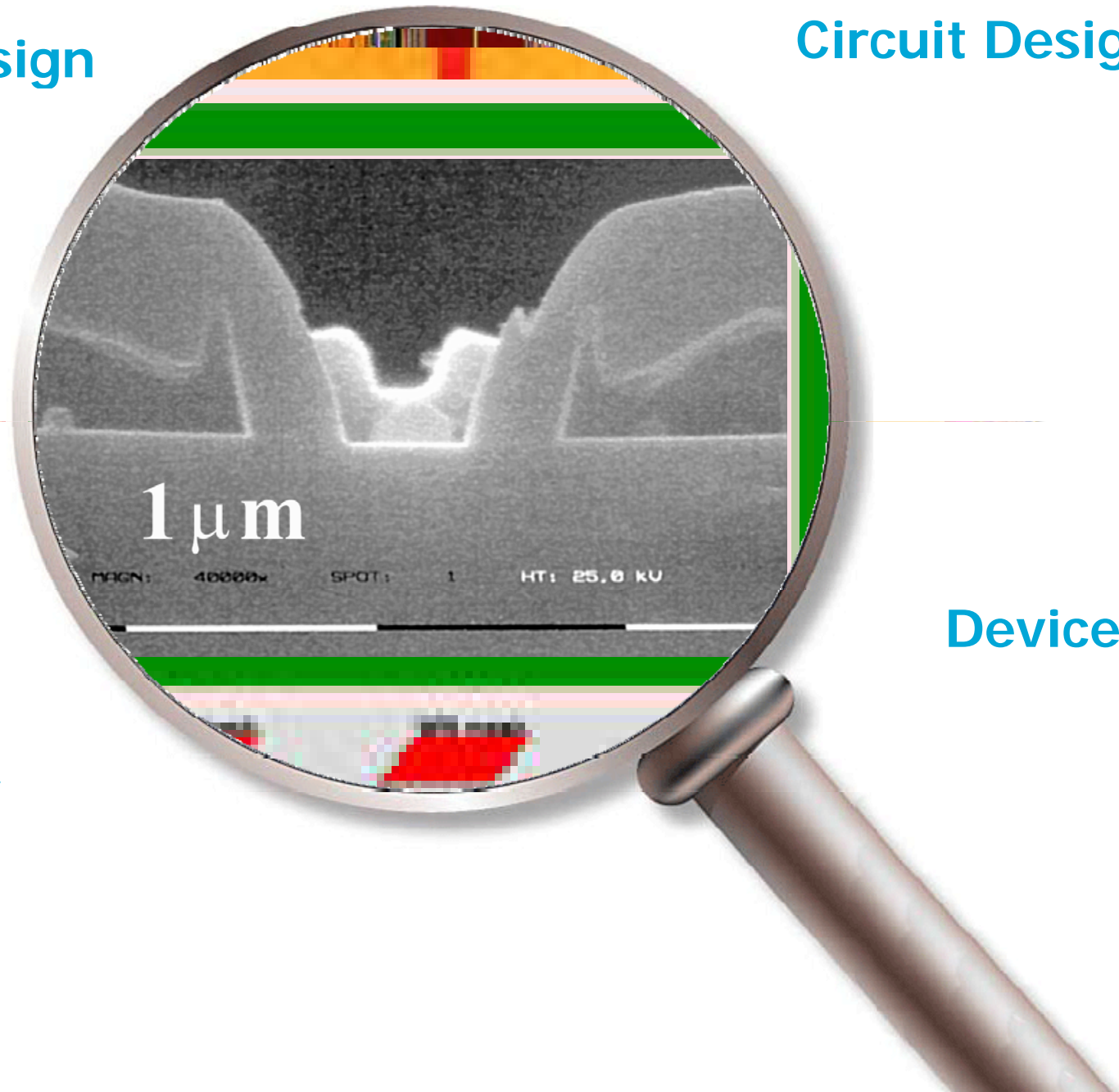
*Digital IC Design*

*N.P. (Nick) van der Meijs*



System Design

Circuit Design



Devices

Process  
Technology  
Physics

[Lina Sarro]

# Design Challenge

## ■ System Complexity

### Dealing with the sheer size of the system

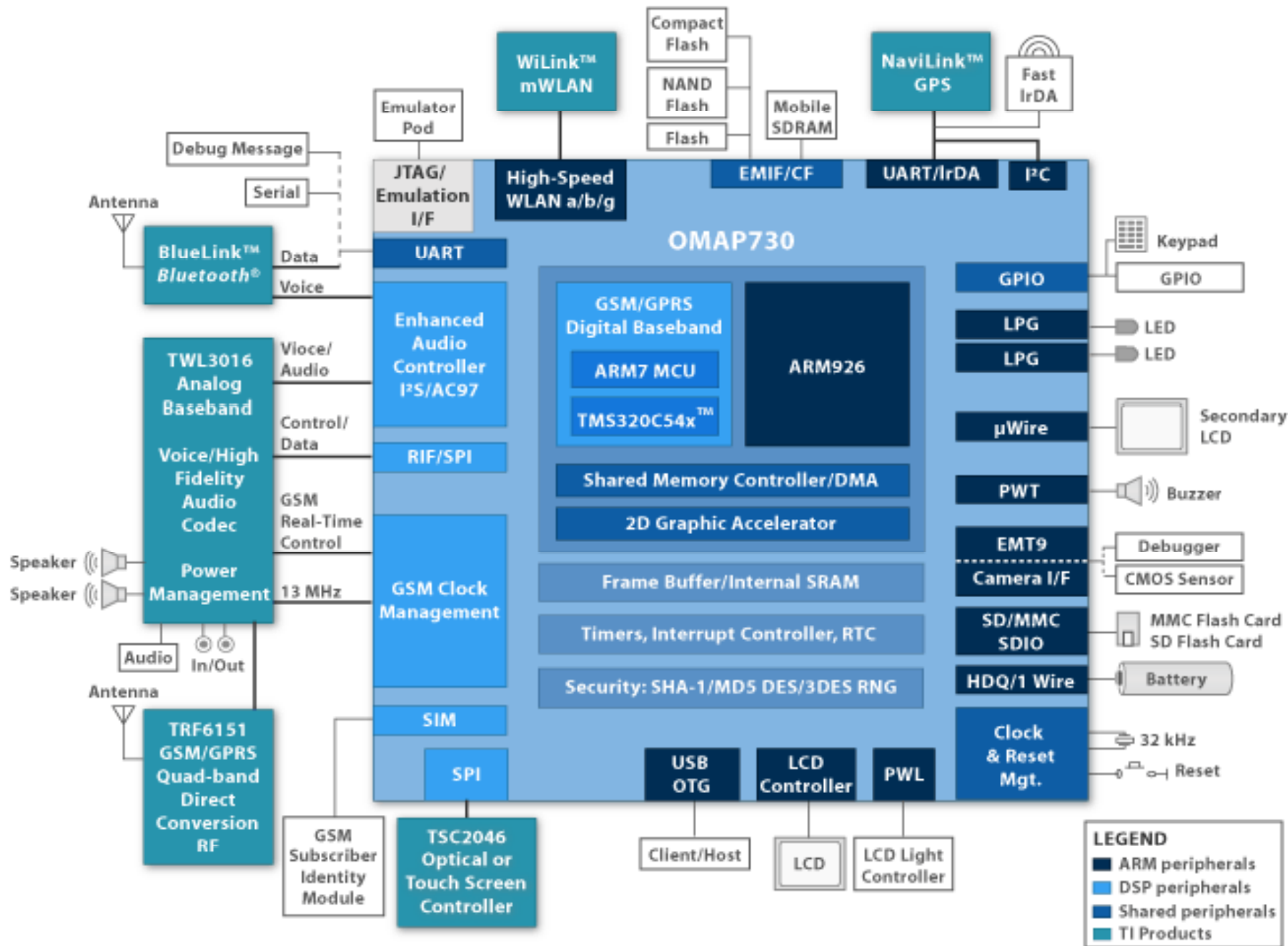
- $> 10^9$  components (transistors)
- Compare boeing 747-400:  $6 \times 10^6$  components
- $\gg 10$  km of interconnect
- Compare boeing 747-400: 274 km wiring, 8 km tubing

## ■ Silicon Complexity

### Dealing with circuit and physical aspects

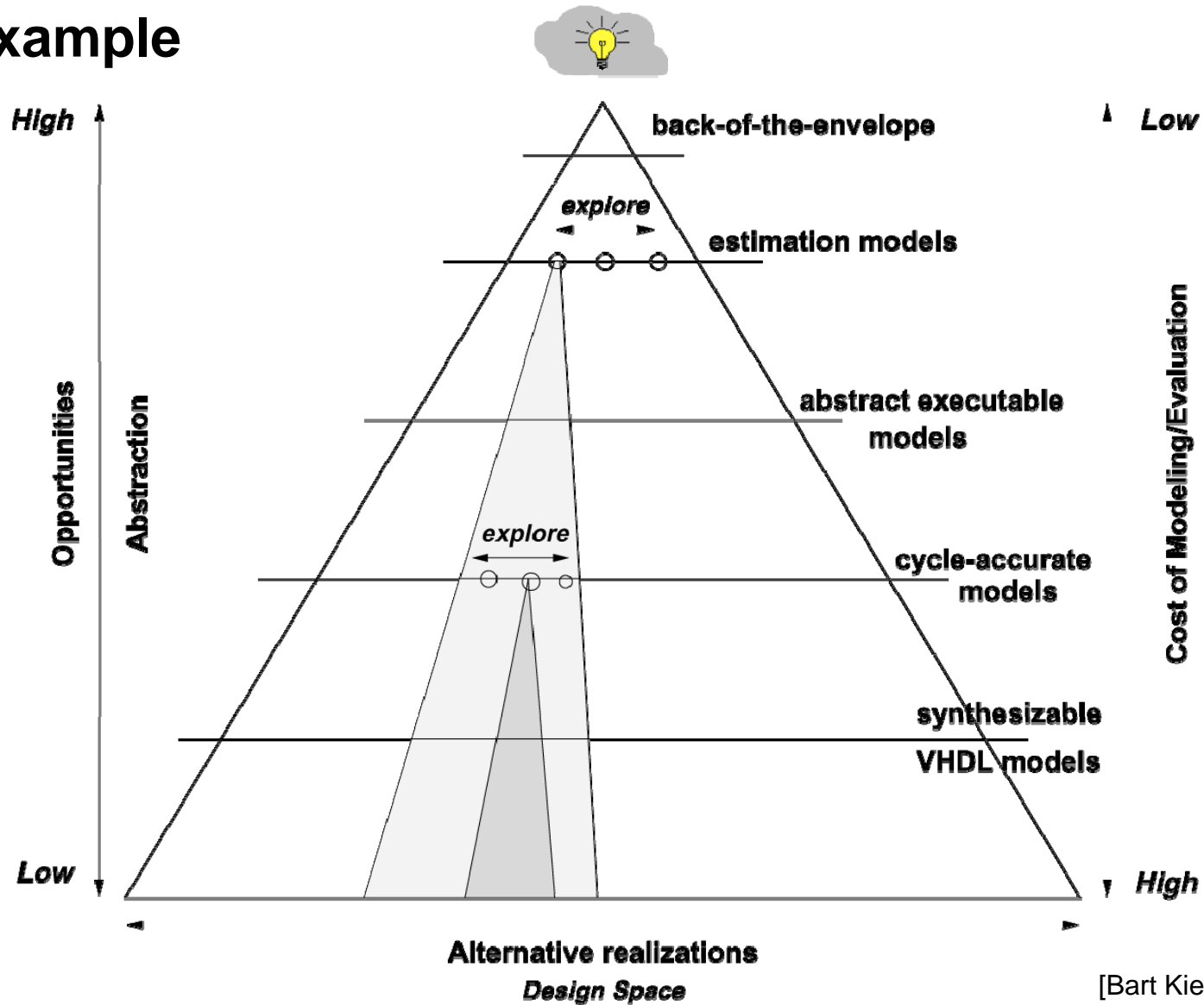
- Features  $< 0.0000001$  m = 100nm
- Actually far from ideal behavior
  - More like building **spaghetti bridges** than steel bridges*
- Lots of unwanted parasitics
- Manufacturing tolerances, ...

[[http://www.boeing.com/commercial/747family/pf/pf\\_facts.html](http://www.boeing.com/commercial/747family/pf/pf_facts.html)]



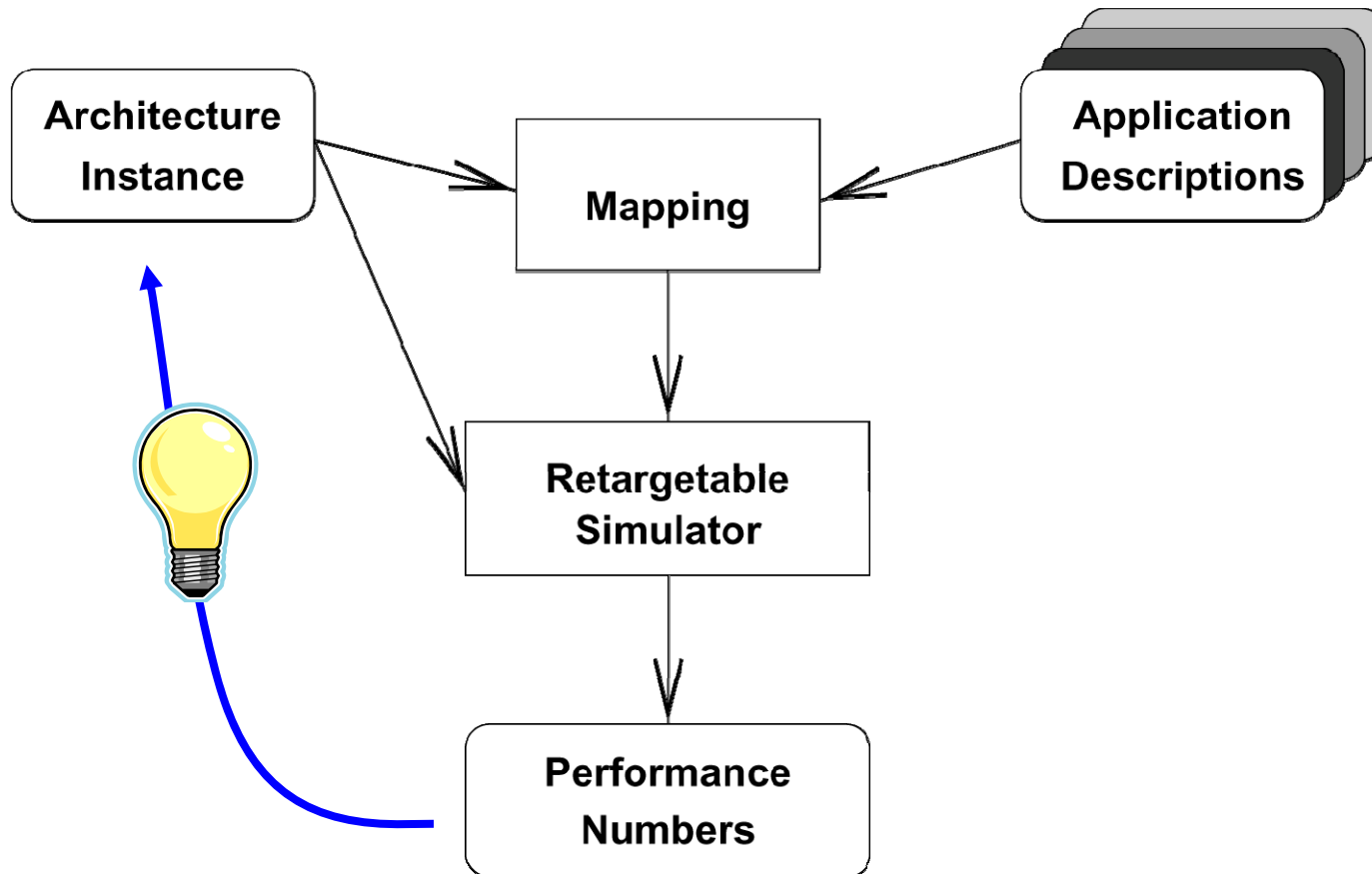
# Dealing with System Complexity (1)

## Example



# Dealing with System Complexity (2)

## Example



[Bart Kienhuis]

# More System Complexity Concepts

- **High-level architecture design**
  - **processors, busses, caches, cache sizes, instruction sets, IP blocks, ...**
- **System on chip design**
- **Cycle-accurate simulation**
- **Network-on-chip, protocols,**

# Course Contents

## ■ **System Complexity (Size of the system)**

- This is not the focus of this course
- But this issue can't be overlooked either – many of the real issues relate to the interplay of system and silicon complexity

## ■ **Silicon Complexity (circuit and physical)**

- This course will focus on these aspects
- Goal is to enable design of large systems
- ... that are not wasteful of resources
- ... that work reliably in face of (almost) failing digital abstraction
- ... that can become competitive products

## Contents (2)

- **How to realize the full potential of advanced manufacturing technologies in realizing digital circuits and systems**
- **Show how circuit-level techniques help improve the overall design properties**
- **Show how properties from physical design create opportunities (and limitations)**

# Digital Electronics

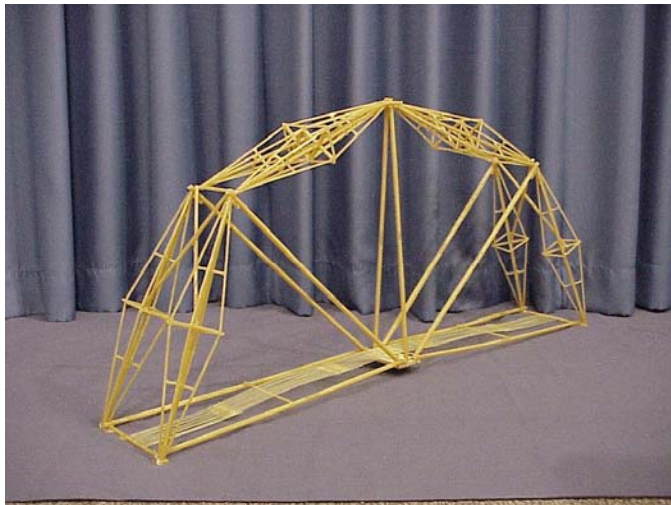
- **Electronics**
  - **Behavior of electronic circuits from an electrical perspective**
  - **Not from an algorithmic perspective**
- **Digital**
  - **Not opamps, but logic gates (etc.)**

# Digital vs Analog

- **Fundamentally, all circuits are analog, they are just ‘overdriven’ to achieve digital behavior**
- **‘Digital’ is just an abstraction**
  - **Way of looking at circuits and signals**
- **Understanding range of validity of digital abstraction is essential**
- **Deep-submicron evokes many unwanted ‘analog’ effects:**
  - **Crosstalk, delay, overshoot, reflection, supply noise, substrate noise, ...**
  - **Digital abstraction has limited (and falling) validity**

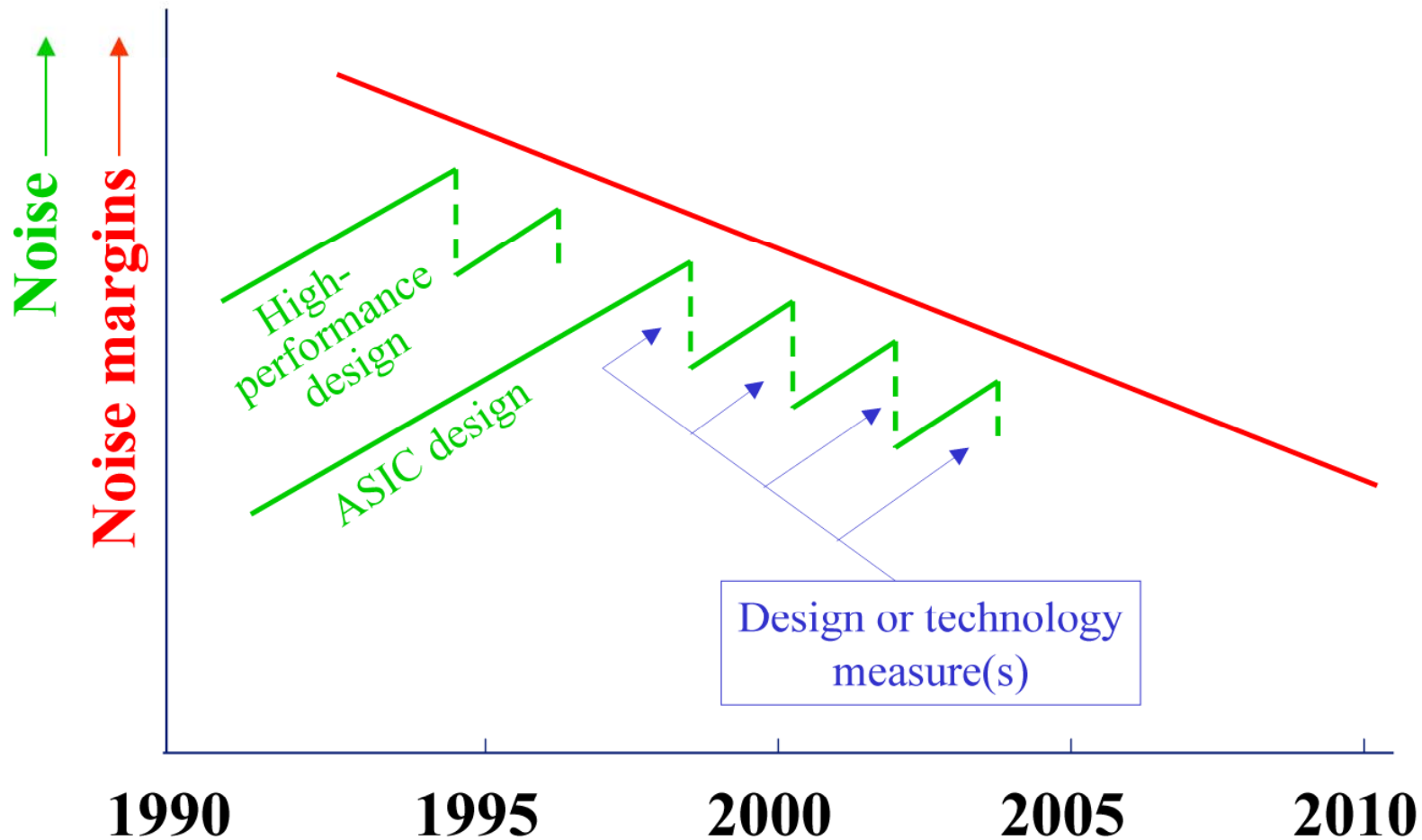
# Scaling

- All features become smaller and smaller
- Smaller means faster but also less ideal
- Deep-submicron design becomes more like building spaghetti bridges than steel bridges



# Example: Voltage Scaling

Noise and Noise margins trends @ nominal voltage



[Slide: Harry Veendrick, NXP]

# Why 'Electronic' insight for VLSI

- **Fundamental insight in exact behavior and opportunities**
- **Deep scaling defeats many standard practices and abstractions**
  - **New design issues arise**

# Why 'Electronic' insight for VLSI

- **Someone needs to design and implement libraries**
- **Creating a model of a (standard) cell and modules requires deep understanding**
- **Library-based design and standard abstractions partially avoided for very high performance designs**

# Why 'Electronic' insight for VLSI

## Troubleshooting

- **Requires in-depth knowledge of all issues involved**
- **of all the circuit bugs, electrical bugs are become more prevalent, and are much harder to find, solve than logical bugs**

# Prerequisites

- **Circuit Theory**
  - Resistor, capacitor, voltage, current, kirchoff laws, power, ...
- **Digital circuits**
  - Boolean logic, logic gates, flip-flops, state-machines, clocking, ...
- **Part 1 of the Rabaey book is essential**
  - MOS devices, technology, ...
  - Will mostly be skipped in this course

# Course Contents

- 1. Inverter – nucleus of digital design**
  - Performance, robustness, area, ...
  - Analysis carries over to other structures
- 2. Complex digital gates**
  - NOR, NAND,
  - Static, dynamic,
  - Sizing for speed, power
- 3. Memory functions (flip flops)**
  - Using stored charge or using feedback
- 4. Implementation strategies**
- 5. Interconnect issues**
- 6. Timing design**
- 7. Building blocks**

# Instructor

## Instructor

Dr. ir. N.P. (Nick) van der Meijs (HB 17.300)

 86258  [n.p.vandermeijs@tudelft.nl](mailto:n.p.vandermeijs@tudelft.nl)

## Lab instructor

Qin Tang (HB 17.050) [Q.Tang@tudelft.nl](mailto:Q.Tang@tudelft.nl)

Amir Zjajo (HB 17.050) [A.vanLoren@tudelft.nl](mailto:A.vanLoren@tudelft.nl)

Javier Rodriguez (TA)

Umanath Kamath (TA)

available: see BB

## Guest instructors

Amir Zjajo, Edoardo Charbon

## Secretary

Minaksie Ramsoekh (HB 17.230)

 81372  [M.W.S.Ramsoekh@tudelft.nl](mailto:M.W.S.Ramsoekh@tudelft.nl)

## Section

Circuits and Systems

<http://ens.ewi.tudelft.nl/>

## Department

Microelectronics & Computer Engineering

<http://me.its.tudelft.nl>

# Course Material

## Book:

Jan M. Rabaey - Digital Integrated Circuits, A Design Perspective, 2<sup>nd</sup> ed, Prentice Hall, 2003 (via ETV)

## Web site:

<http://cas.et.tudelft.nl/~nick/courses/digic>

Bi-directional link with blackboard

Announcements, etc.

Lecture slides (!)

Project data

Blackboard Discussion Forum (!)

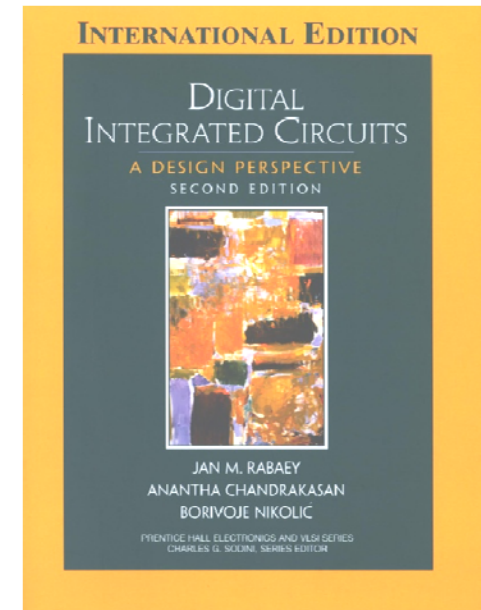
## Syllabus:

website

## Slides / Presentation Material:

Website – published, usually **after lecture**,

Last year's website, slides still available



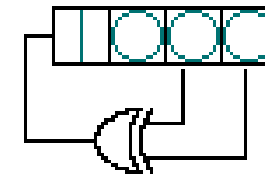
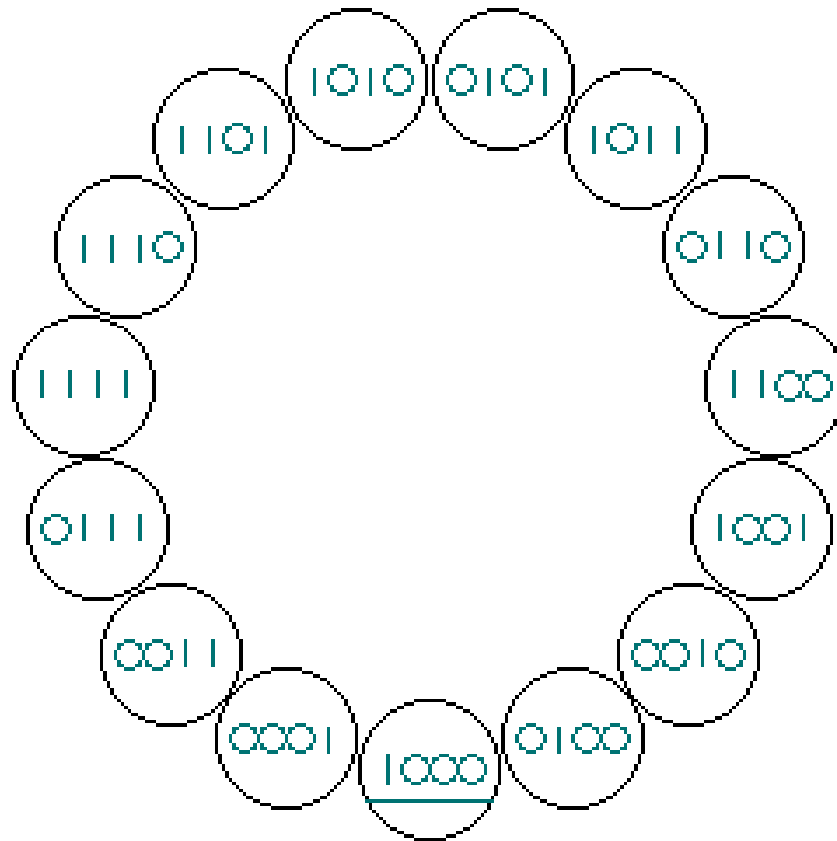
# Practice Exercises

- **Spectre Simulation exercise**
- **Transistor, Nand gate layout using Cadence**
- **Instructions next Thursday**
- **Work in teams of 2**
- **Need to be completed**
  - **Will be checked**
  - **Not graded**

# Project

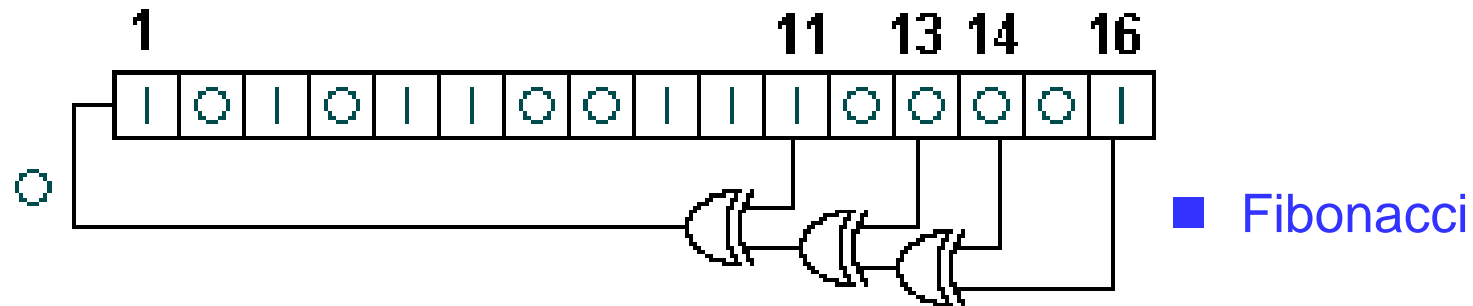
- **Pseudo Random Number Generator (PRNG)**
- A 'counter' producing an output sequence that **approximates** the properties of **random numbers**
- Pseudo random sequences have **many applications**
  - Spread spectrum communication
  - Whitening
  - Monte-Carlo simulation
  - Stream ciphers
  - Test pattern generation
  - ...

# 4-bit Fibonacci LFSR

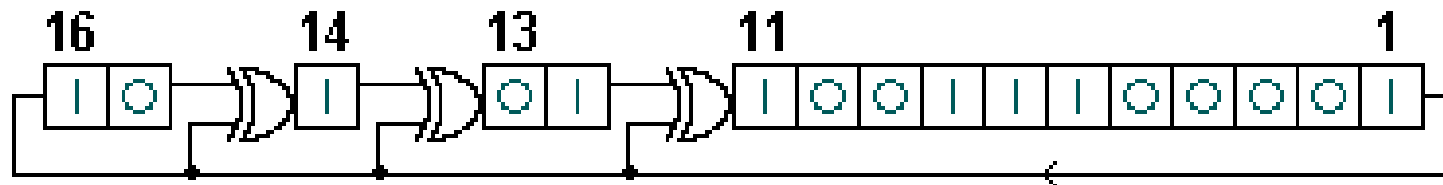


[http://en.wikipedia.org/wiki/Linear\\_feedback\\_shift\\_register](http://en.wikipedia.org/wiki/Linear_feedback_shift_register)

# Fibonacci vs. Galois Style



Can expect differences in speed/power tradeoff



■ Galois

# Project Information

- **Work with teams of 2**
- **8-bit, fixed speed, optimize power, area**
- **No VHDL, no layout, “just” SPECTRE, corner-analysis, ...**
- **documentation is important**
- **Start of project before spring break**
- **Final presentations in week 1 of Q4 (tentatively)**
- **(previous year’s projects: time-to-digital converter, thermometer to binary decoder)**

# Teams

- **Make teams now**
- **List teams, students looking for teams, next Thursday.**
- **Completion with help from us**

# Agenda

- Lectures on Mon 5<sup>th</sup> + 6<sup>th</sup> (@ IDE Wim Crouwel, here) and Thu 7<sup>th</sup> + 8<sup>th</sup>, (@ EWI - room B)
- Handout/web exercises, to be discussed during lecture
- Lab exercises / Design project
  - Bonus points to be awarded for best designs
  - Includes report and presentation
  - Cadence design system
  - Details will follow
- **Written exam April 16, 2 pm – 5 pm**  
open book
- Mark determined for 50% by exam, 50% by design project

# Agenda

- Rest of today's lecture – Chapter 3 (Devices)
- Will not be presented:  
Introduction – Chapter 1  
Process – Chapter 2

Ch 1 – 4:

Required reading/studying for Mon Feb 13

**In-class test on Chapters 1 – 4 on Mon Feb 13**

## ■ Questions?

