

Coherent Interconnect/Substrate Modeling Using SPACE - An Experimental Study

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Abstract

The functionality of modern IC's increasingly suffers from substrate noise. Digital transistors switching at high frequencies are known to induce substrate noise through their bulk contacts. In addition, interconnect carrying aggressive, high-frequency signals is known to induce substrate noise through its capacitive coupling with the substrate. In this paper, we describe how our layout-to-circuit extractor SPACE builds a coherent interconnect/substrate model from a layout. The result is a comprehensive circuit model which can immediately be simulated by a regular circuit simulator. We evaluate our modeling approach by extracting a ring-oscillator layout and simulating the resulting circuit with HSPICE. We have done extractions under varying conditions; the simulation results give practical insight into relevant substrate noise phenomena.

1 Introduction

With the increasing clock frequencies and integration densities, present-day IC's suffer in an increasing way from parasitic coupling effects via the substrate. These coupling effects may cause noise, originating from one location on an integrated circuit, to propagate "subliminally" to another part of the circuit, where it may have a fatal influence on circuit behavior. Typical examples of this are found in mixed analog-digital circuits, where noise that is generated in digital parts may propagate via the substrate to analog parts like amplifiers (see e.g. [1, 2, 3]). Alternatively, in fully digital circuits, substrate noise may influence the behaviour of the clock generator (typically a PLL), causing fluctuations in the clock frequency (clock jitter).

Substrate noise is known to be a highly complex phenomenon in which many factors play a role. These factors include on-chip effects like noise injection through the bulk contact of digital transistors switching at high frequencies, or through capacitive coupling from interconnect carrying aggressive, high-frequency signals. Additionally, the substrate doping profile and the floorplan of the chip determine how the noise propagates through the substrate and where it is picked up. Finally, off-chip effects like inductance from the bond wires or the package may also play a role: the low-pass characteristics of the inductance cause sharp switching spikes in e.g. the supply/ground lines to be reflected back into the chip where they may inject into the substrate through e.g. biasing connections to the substrate or the wells.

Even though this brief summary of substrate-related ef-

fects is not complete, it does indicate that any modeling approach aimed at predicting and/or analyzing substrate noise phenomena should be coherent and comprehensive.

Fortunately, some hierarchy is possible. At device level, the noise behaviour/sensitivity of transistors is studied in the field of device physics, and is captured by accurate behavioral transistor models like the SPICE BSIM3 models. At the intermediate level, i.e. chip level, the noise behaviour of the chip, including injection from the interconnect, propagation through the substrate doping profile, and floorplan dependency, is studied in the field of physical verification, resulting in simulation, modeling and extraction tools like layout-to-circuit extractors. At package level, the (inductive) characteristics of the bond wires and the chip package can be determined through package modeling and simulation tools.

When a common format (e.g. a SPICE netlist) is used for representing the models at the three different levels, then the separate models can be assembled into one comprehensive model that, in principle, allows for a representative simulation of the entire chip. However, depending on the complexity of the chip, and the required accuracy of the models, full-chip simulations may not always be feasible. Nevertheless, modeling and simulation are important parts of a design flow.

In this paper, we will summarize a methodology for modeling substrate noise effects at the chip level. The method allows coherent modeling of the interconnect and the substrate, including distributed RC modeling. The method has been implemented in the SPACE layout-to-circuit extractor [4, 5], and results in a comprehensive circuit model that can be simulated using a circuit simulator like HSPICE. We will show a representative application of the method by using SPACE on a simple 9-section ring-oscillator design, and simulating the resulting circuit model. The simulation results provide practical insight in some relevant substrate noise phenomena.

The paper is organized as follows: Section 2 will sketch the mechanism that causes substrate noise to be injected through the interconnect, and will summarize the modeling methodology as implemented in SPACE. Section 3 presents our simulation results, and, finally, Section 4 presents our conclusions.

2 Modeling Approach

It is well known that substrate noise can originate from the bulk connection of transistors and from noisy supply/ground lines (i.e. connected to the outside world through a parasitic package inductance) that are connected

to the substrate and the wells. However, these are not the only elements on a chip that may cause substrate noise. Something similar occurs for interconnect, where the potential-field surrounding a charged piece of interconnect will also affect the charge distribution in the substrate. In terms of modeling, this potential field can be represented by a capacitor being placed between the piece of interconnect and the substrate. This capacitor may cause significant crosstalk from the interconnect to the substrate as signal frequencies become higher. As such, interconnect also contributes to substrate noise.

The work presented in [6] already showed the importance of simultaneous interconnect-substrate modeling for a special HF device-calibration structure. The models in the paper were constructed under prototyping and evaluation conditions, but showed that only a combined interconnect/substrate model behaved similarly to measurements on the fabricated structure. This observation worked as an incentive to develop a more general approach for coherent modeling.

From a modeling point of view, the most important difference between the main types of noise sources is the area where they influence the substrate.

1. For the transistor, the influence area is very well-defined; it is situated immediately underneath the transistor itself, i.e. underneath the gate, source and drain areas.
2. Similarly, biasing of the wells and the substrate takes place through via-connections to the (noisy) supply lines. Vias also have a clearly defined area where they influence the substrate.
3. Interconnect, however, influences the substrate in a more indirect way through a potential field, which hampers a clear definition of an influence area.

In the first two cases, it is possible to accurately define terminal areas on top of the substrate, through which the interaction with either transistor or via takes place; this facilitates the construction of the substrate model. In the third case, however, defining a terminal area is less straightforward and subject to some approximations.

During operation, the interconnect will radiate an electric field which affects the charge distribution in the substrate. This is equivalent to a distributed capacitance between the interconnect and the substrate, which can be approximated with a lumped model as in Figure 1.

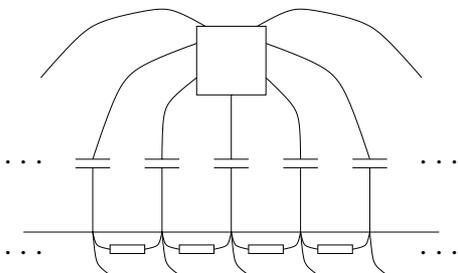


Figure 1: Cross-section of a wire with a lumped model for the interaction with the substrate.

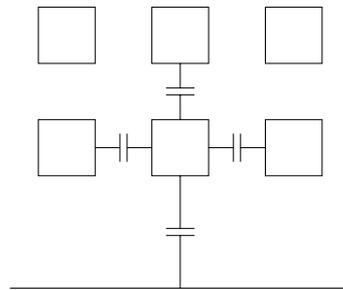


Figure 2: Cross-section of a wire with coupling to the substrate in a practical situation.

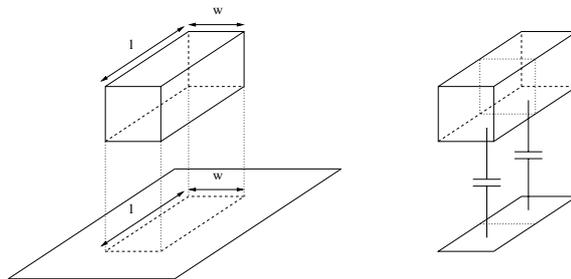


Figure 3: Left: Shadow contact underneath interconnect wire; Right: Lumped modeling approach for long wires.

It shows that in reality the influence area on the substrate can not be considered a terminal with fixed dimensions, but should be seen as a distributed interaction between the interconnect-to-substrate capacitance and the substrate.

Our modeling approach works from the observation that the largest portion of the capacitance will be concentrated directly below the wire because (1) the distance to the substrate is shortest at that position and (2) in practical situations the surrounding of the noise generating wire will be shielded by other wires, see Figure 2. As such, it is assumed that the interaction between interconnect and substrate mainly takes place directly underneath the wire. This allows for a straightforward definition of the influence area as the "shadow" of the wire (see Figure 3; left). This shadow, by default, has the same length and width dimensions as the wire, but it is also possible to choose it somewhat larger to include some of the fringe effects shown in Figure 1.

There are various computational approaches to acquire the wire-to-substrate capacitance and the substrate resistance. Our extractor can model capacitance and substrate resistance using either the 3D BEM for accurate computation or a 2D interpolation method based on area-perimeter calculations for fast computation.

When a wire is relatively long, there will also be distributed effects along its length. Therefore, our modeling methodology also applies lumped modeling along the length of the wire (see Figure 3; right). Thus, smaller portions of the interconnect capacitances are then connected to smaller substrate areas.

For each substrate area, a node is created in the final netlist, as shown in Figure 4. The substrate capacitance that is computed for the part of the interconnect that is

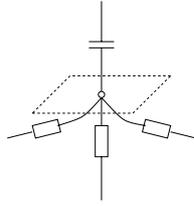


Figure 4: Single node model for a substrate terminal.

above the area, is attached to this node. The substrate resistances that are computed for the substrate underneath the area, are also attached to this node. In this way, a representative and comprehensive electrical network is created from the original structure. This electrical network (possibly after model reduction) can then be simulated using a simulator like HSPICE.

3 Results

The layout that we work from is the 9-section ring oscillator from Figure 5. The inner ring consists of polysilicon interconnect which carries the actual oscillating signal. The outer ring is a ground line that is situated in the first metal layer. The outer ring is also connected to the substrate through a via halfway along the left edge. On the right, there is a sensor node placed on the substrate just outside the outer ring. The whole structure is situated on top of a p-type substrate with a conductivity of 10 S/m. All transistors have 250nm gatelength. The transistors connected to the outer ring are n-channel enhancement MOSFETs; they have a direct connection to the substrate immediately underneath their gate. The transistors connected to the inner supply line, V_{dd} , are p-channel enhancement MOSFETs and they are embedded in an n-well. These transistors have a connection to the substrate through the junction capacitance between the n-well and the p-substrate.

To study the substrate-noise contributions of the transistors and the interconnect separately and simultaneously, we used 3 different settings for our extractor. In the first case, only the transistors were connected to the substrate, while the interconnect capacitances were connected to a (fictitious) ideal ground. In the second case, we chose

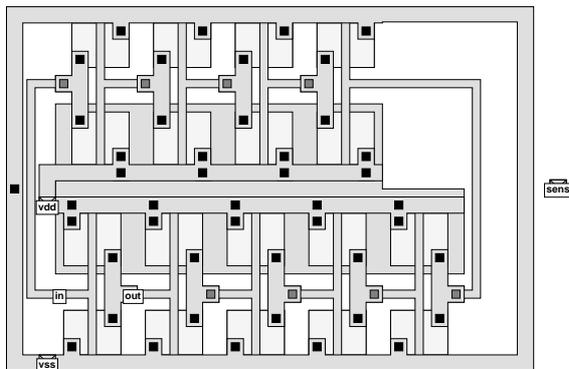


Figure 5: 9-section ring oscillator with sensor node

the converse situation, where only the interconnect capacitances were connected to the substrate, and the bulk contacts of the transistors were connected to either V_{dd} or V_{ss} , depending on their type. In the third case, we chose both transistors and interconnect capacitances to be connected to the substrate.

For these experiments, we chose the 3D BEM modeling method for both capacitance and substrate. After the extraction, we simulated the resulting netlist with HSPICE. Our extractor, SPACE, allows to recognize different transistor types, and include their HSPICE model in the final netlist. The transistor model that we use is a commercially available level 49 model (belonging to the class of BSIM3 models), which was chosen because of its good numerical stability and realistic behaviour with respect to the switching noise visible at its bulk contact.

The results can be seen in Figure 6, which shows the signal visible at the sensor node for the 3 different situations described above. The oscillator frequency is approximately the same under all 3 circumstances: 925 MHz. We observe from the figure that the interconnect is a much stronger noise source than the transistors. From this figure, we can conclude that including interconnect-to-substrate effects into our model has an important impact on the shape and the amplitude of the substrate noise signal, but not on the functionality of the oscillator itself.

The large noise-contribution of the interconnect as mentioned in the previous paragraph may be caused by the signal-carrying interconnect being mainly in the polysilicon layer, which is much closer to the substrate (600nm) than e.g. the first metal layer (1700nm), or the second metal layer (2800nm). We have verified this by modifying our design such that the major part of the signal carrying interconnect (but also the supply lines) was in the first or the second metal layer (except near the gates of the transistors). The results for this experiment can be found in Figure 7. The figure shows that switching from poly to metal1 will significantly reduce the amplitude of the noise, but switching from metal1 to metal2 has little effect. This observation can be explained from physics: a parallel plate approximation holds for short distances between the interconnect and the substrate, but at longer distances the capacitance value converges to a constant value. The constant value to which it converges can be interpreted as the capacitance of a conductor (possibly part of a group of conductors) in infinite space with the ground at infinity. Apparently, switching from poly to metal1 is still near the parallel plate approximation, while switching from metal1 to metal2 is already in the convergence region.

As we have seen in Figures 6 and 7, the amplitude of the noise can be significant. However, in these experiments, only the single oscillating signal was responsible for the noise. Under realistic circumstances, the noise will be generated by many more (weakly- or uncorrelated) signals, which generally leads to noise averaging. The following experiment will illustrate this phenomenon.

In this case, we duplicate the ring-oscillator from Figure 5 in the y-direction, and also move the sensor node in the y-direction. We now have two identical ring-oscillators near to each other, with a single sensor node halfway along

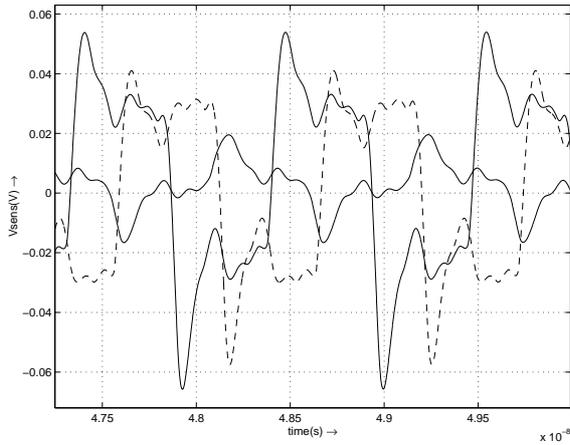


Figure 6: Substrate noise on sensor node. Small amplitude (solid line): transistors only; Larger amplitude (dashed line): interconnect only; Largest amplitude (solid line): both

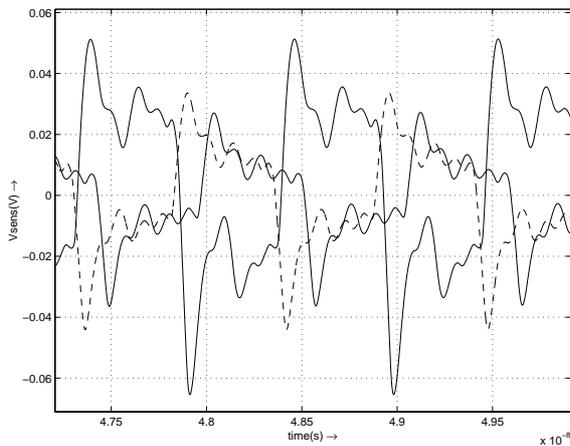


Figure 7: Substrate noise on sensor node for interconnect in poly, metal1 and metal2. Largest amplitude (solid line): poly; Smaller amplitude (dashed line): metal1; smallest amplitude (solid line): metal2

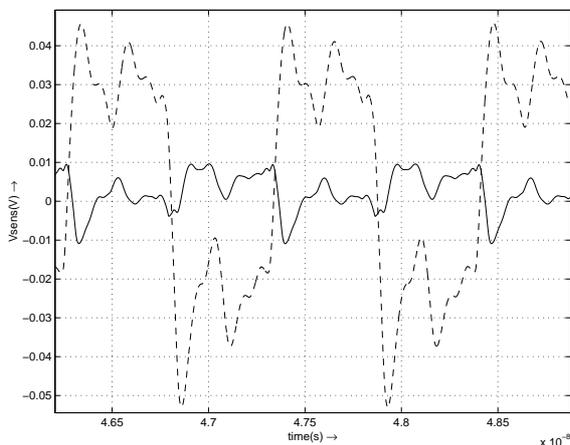


Figure 8: Substrate noise on sensor node for double oscillator. Dashed line: oscillators are in phase; Solid line: oscillators are in anti-phase

the right edge. By choosing the initial conditions for each ring-oscillator either the same, or opposite, we can have the oscillators work either in phase or in anti-phase. The noise signal for each case is displayed in Figure 8. It clearly shows that averaging may play a significant role in the resulting shape and amplitude of the noise signal.

4 Conclusions

The adverse effect of substrate noise on the functionality of modern IC designs is well known. Efficient modeling methodologies aimed at predicting substrate noise effects play an ever important role in design flows. Many factors play a role in substrate noise and therefore, the modeling problem requires approaches at different levels: device-, chip-, and package level.

In this paper we summarized a methodology for coherent interconnect/substrate modeling at the chip level. The method has been implemented in the SPACE layout-to-circuit extractor and has been used to extract a ring-oscillator layout. The extractions took place under varying circumstances, and resulted in electrical circuit models which were simulated with HSPICE. The simulation results provided practical insight in the following phenomena: (1) Substrate noise generated by transistors and interconnect separately and simultaneously; (2) Noise reduction by placing interconnects in higher metal layers; (3) Noise averaging due to noise generators working in phase or in anti-phase.

The algorithms and modeling methodologies developed for, and implemented in, SPACE have proven to be more efficient than those used in many industrial tools.

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