Extracting Simple but Accurate RC Models for VLSI Interconnect*

A. J. van Genderen and N. P. van der Meijs

Delft University of Technology
Department of Electrical Engineering
Mekelweg 4, 2628 CD Delft
The Netherlands

Abstract

This paper describes a new method to find RC models for (non-orthogonal) interconnections in VLSI layouts, including resistances as well as ground and coupling capacitances.

The method starts with the construction of a finite element mesh for the interconnection polygons. Resistances are assigned to the edges of the mesh, and capacitances to the vertices. Then, all internal nodes are eliminated by a novel and efficient node reduction algorithm. This algorithm preserves the Elmore time constants between the remaining nodes, without actually computing them. The resulting network accurately reflects the electrical properties of the distributed RC interconnections, and can efficiently be simulated. All steps are executed in a single scan-line sweep over the layout. The expected time complexity of the method is $O(N)$, where N is the number of contour edges of the interconnection polygons.

Introduction

Parasitic resistances and capacitances of interconnections heavily influence the behavior of VLSI circuits. In order to verify a circuit for these influences by means of simulation, lumped RC models for the interconnections are needed. Several extractors have been developed that can accurately extract resistances and capacitances from VLSI layouts [1, 2]. However, to combine resistances and capacitances into one model, heuristics like dividing the capacitance in equal parts over the nodes of the lumped resistance model are usually being used (see figure 1).

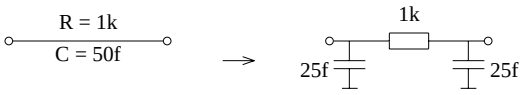

Figure 1. Heuristic to combine distributed resistance and capacitance into one lumped model.

Although resistance and capacitance values themselves are accurate, the lumped model as a whole can still be inaccurate then.

* This research was supported in part by the commission of the EC under ESPRIT contract 991 and by the FOM under IOP-IC contract 45.009.

The circuit extraction method as presented here uses a new strategy that allows accurate modeling of both the resistive and capacitive effect, as well as their combined effect. It uses finite elements to construct from the layout a fine RC mesh that models resistive and capacitive effects in detail, and then applies a node reduction technique to find the final RC network. The nodes of the final network correspond to the terminals of the interconnect, but depending on the desired trade-off between simulation accuracy and simulation time, other nodes can be retained as well. The Elmore time constants [3] between the output nodes are unchanged with respect to their value in the fine RC mesh. This will guarantee (see also [4]) that the electrical transfer function of the final network closely matches that of the fine RC mesh and, consequently, that of the distributed RC interconnect.

The extraction method as described here is simple and straightforward, it can handle non-orthogonal layouts, and provides both ground and coupling capacitances.

As a scanline is swept over the layout plane, the different steps of the method are executed in one pass. Finite elements and the RC mesh are locally constructed from the layout description, and nodes are eliminated as soon as all resistances and capacitances for a node are known. This results in low time and space complexities.

Resistance calculation

Using a scanline algorithm, the layout is subdivided into a set of non-overlapping trapezoids, such that every trapezoid has a unique mask combination. The trapezoids that contain interconnect are then subdivided into boxes and triangles as in figure 2.

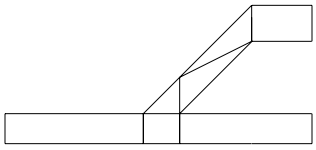

Figure 2. Decomposing a layout polygon into uniform boxes and triangles.

These boxes and triangles form a finite element mesh, which is interpreted as a resistance network by assigning resistances to the edges [5, 6]. This is illustrated in figure 3.

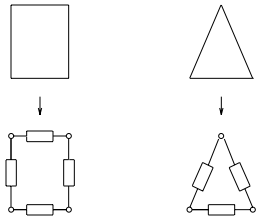

Figure 3. Assignment of resistances to edges.

When

$$\sigma = \textit{conductivity of material}$$
$$A = \textit{area of element}$$

the conductance G_{ij} (= $1/R_{ij}$) between two nodes i, j of a triangle which has nodes i, j, k, is given by

$$G_{ij} = \sigma \frac{(x_k - x_i)(x_k - x_j) + (y_k - y_i)(y_k - y_j)}{4A} \qquad (1)$$

For a box, the conductance between two nodes i, j is given by

$$G_{ij} = \begin{cases} \sigma \dfrac{(x_i - x_j)^2}{2A} & \textit{if } y_i = y_j \\ \sigma \dfrac{(y_i - y_j)^2}{2A} & \textit{if } x_i = x_j \\ 0 & \textit{otherwise} \end{cases} \qquad (2)$$

which is equivalent to using the length-width ratio of the box.

Capacitance calculation

The capacitance of interconnects is calculated using a perimeter/surface method [7], for the boxes and triangles constituting the finite-element mesh. Then, these (distributed) edge and surface capacitances are converted into lumped capacitances that are connected to the vertices of the mesh. Edge capacitances are equally divided over the two vertices that are connected to the edge, while surface capacitances are divided according to the areas that are bounded by the lines of gravity of the boxes and triangles. The latter is illustrated in figure 4.

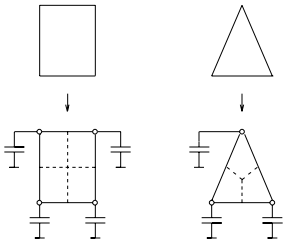

Figure 4. Assignment of surface capacitances to vertices.

Node reduction

As resistances are assigned to the edges and capacitances to the vertices of the finite element mesh, an RC network results. For example, the piece of interconnect of figure 5(a), which has three terminals and a distributed ground capacitance, will give the RC network of figure 5(b).

This network is now transformed into a network that has a smaller number of nodes. Figure 5(c) shows the network that is the result of such a simplification for the RC network of figure 5(b). The transformation is done by an algorithm that repeatedly eliminates one node from the network until there are no more nodes to be eliminated. Each elimination step preserves the Elmore time constants between the other nodes, without actually computing them.

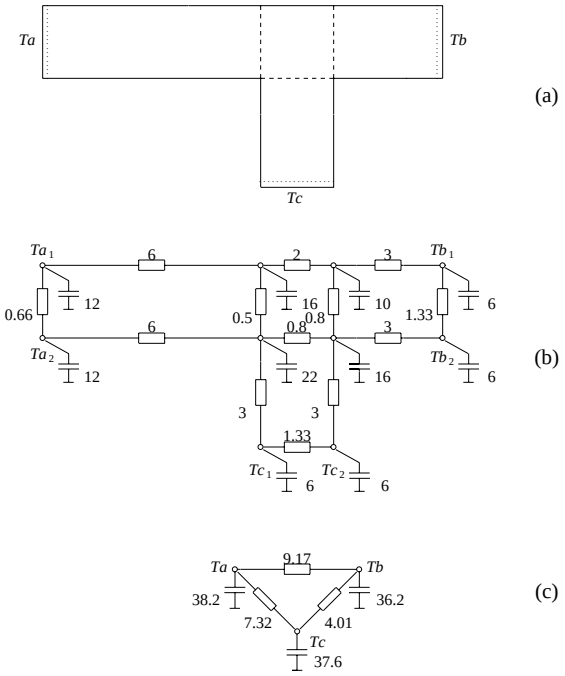

Figure 5. Interconnect polygon subdivided into finite elements (a), the resulting RC mesh model (b) and the final pi-model (c).

To describe how the algorithm works, consider a node of an RC mesh as in figure 6(a), which has one capacitance and several resistances connected to it.

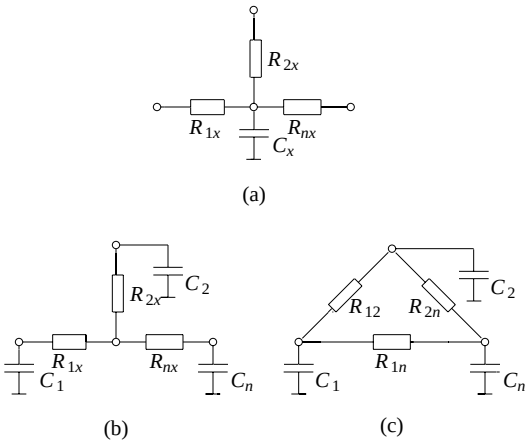

Figure 6. Node elimination by capacitance redistribution (b), and Gaussian elimination (c).

We first divide the capacitance C_x of node x over the nodes i that are connected to node x by means of the resistances R_{ix}. Each node i is assigned a capacitance

$$C_i = \frac{G_{ix}}{\sum_{all\ k} G_{kx}} C_x \qquad (3)$$

To see that the Elmore time constants of the nodes do not change, notice that due to (3), the total capacitance does not change and for each pair of nodes i, j, we have

$$\frac{C_i}{G_{ix}} = \frac{C_j}{G_{jx}} \tag{4}$$

or alternatively

$$R_{ix}C_i = R_{jx}C_j \tag{5}$$

For a tree network the proposition can then easily be verified. For a general RC network containing resistance loops, it should be realized that according to [8] this network can always (by means of tree decomposition and load redistribution) be interpreted as a tree network.

The capacitance redistribution step can also be performed for coupling capacitances. Although the Elmore time constant is not defined for such capacitances, this can intuitively be justified with the aid of the superposition principle.

After the capacitance distribution, the node is removed by a Gaussian elimination step:

$$G_{ij} = \frac{G_{ix}G_{jx}}{\sum_{all\ k} G_{kx}} \tag{6}$$

This again does not change the Elmore time constants between the remaining nodes.

Additionally, nodes of one terminal (which are on the same potential) are collapsed.

Implementation

The algorithms explained in this paper have been incorporated in a newly implemented circuit extractor for MOS integrated circuits. The extractor is scanline based; it executes all steps of the method while scanning the layout from left to right.

During the scan, trapezoids are created and passed to an element recognition routine. When a trapezoid contains interconnect, it is split into boxes and triangles, and the edge resistances and the vertex capacitances are computed. When all resistances and capacitances for a vertex are found, the vertex is eliminated in order to reduce memory requirements. Using a perimeter/surface method, this can be done as soon as the scanline has passed all boxes and triangles of which the vertex is part of.

Complexity

The stateruler generates boxes and triangles in a constant time per box/triangle[9]. Resistance and ground capacitance calculation for a box or triangle can also be performed in a constant time.

Elimination of a node takes $O(R^2+CR)$ time, where R and C are the number of resistances and capacitances connected to the node respectively, perhaps after some other node eliminations. Since resistors do not bridge conductors, $R \le r-1+x$, where r is the number of nodes on the same trapezoid(s) as the node to be deleted, and x is the number of external nodes (nodes that are retained in the final network) on the same conductor but to the left of the node to be deleted. In practice, this term is for most conductors bounded by a small constant. If no coupling but only ground capacitances are extracted, $C \equiv 1$, and the elimination of a node takes constant time in the expected case.

Since the expected number of nodes is proportional to the number of boxes and triangles, which is proportional to the number of contour edges denoted by N, we arrive at a expected-case time complexity of $O(N)$.

When extracting coupling capacitances the number of coupling capacitances for a node is not a priory known and C can in principle obtain an arbitrary high value. However, the expected number of coupling capacitances for a node does not depend on the size of the input, but only on some local geometrical properties and C will be be reasonably bounded in practice. Also, heuristics like neglecting small coupling capacitances further confine the value of C, this way reassuring the expected time complexity of $O(N)$.

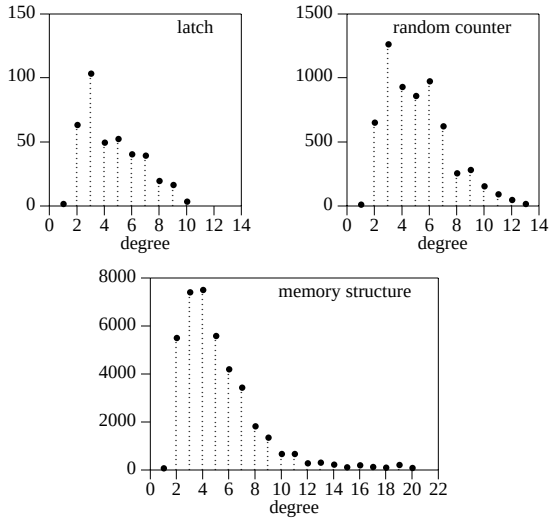

Figure 7. The number of nodes (vertically) as a function of the degree of the node for three different designs.

Some experimental support for the analysis in this section was obtained by adding instrumentation code to our circuit extraction program. The results are presented in figure 7, showing the number of nodes as a function of R, (also called the degree of a node), which is the number of resistances connected to the node just prior to its elimination. This data was obtained for three NMOS designs of increasing complexity while extracting ground capacitance and poly and diffusion resistance. Coupling capacitance and metal resistance extraction was inhibited. Under these conditions, the degree of a node fully determines the cost of eliminating the node.

Although the maximum degree of all nodes in a design seems to increase with the size of the design, a further analysis shows that this effect is relatively insignificant. More specifically, the cost of eliminating a node with degree R (and without coupling capacitance) is proportional to R^2+R, and the total cost of eliminating all nodes is proportional to

$$C_{total} = \sum_{r=1}^{R_{max}} f(r)(r^2+r)$$

where $f(r)$ is the number of nodes with degree r. When this cost is normalized with respect to N, the number of contour edges in the design, a behavior only slightly worse than linear can be observed as shown in the following table:

design	number of contour edges N/1000	cost of node elimination C_{total}/1000	C_{total}/N
latch	0.20	11	55
random counter	2.9	218	75
memory structure	20.5	1800	88

Accuracy

To illustrate the accuracy of the method, an RC model for the piece of VLSI interconnect as shown in figure 8 was extracted.

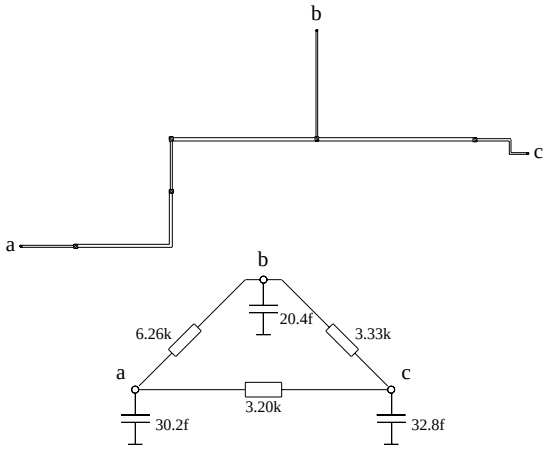

Figure 8. An VLSI interconnection and its extracted model.

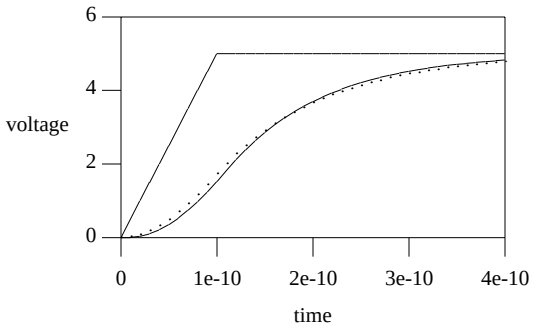

Figure 9. Voltage at node 'c' when a ramp input voltage is applied to 'a'.

In figure 9 the output voltage at node 'c' is plotted (dotted curve) when the RC model is simulated with the circuit simulator SPICE and a ramp input voltage is applied to node 'a'. The exact solution for the voltage at node 'a' - which has been approximated by simulating a model for which nodes has been retained at each contact - is also given in figure 9 (solid curve). A comparison between both results shows that a reduction of the number of nodes from 8 in the detailed model to 3 in the extracted model has only a small influence on the output voltage waveform. Due to the absence of the higher order time constants the output voltage for the simple model rises somewhat faster, but due the property that the Elmore time constants are equal, the net area between both curves in the figure will be zero. Especially around 2-3 Volt, which is important as the switching region for transistors, the voltage waveform of the extracted interconnection model closely matches the exact voltage waveform.

Discussion

We have described a new method for extracting accurate lumped RC models for interconnections in VLSI layouts. Part of this method is a novel node reduction technique that does not change the Elmore time constants. The usefulness of such a node reduction technique has already been recognized in [4], where it is used as a post-processing step after circuit extraction. Our node reduction technique however is fully integrated in the extraction method, and is simpler and more general. It can handle networks containing resistance loops and coupling capacitances.

In fact, our extraction method can be considered as an extension towards mixed resistance/capacitance extraction of the resistance extraction method as described in [5]. Apart from also handling capacitances, the other differences with [5] are (1) our method also handles non-orthogonal layouts, and (2) instead of using explicit matrix operations for the Gaussian elimination step, our method exploits the locality of each node elimination by taking into account only the elements that are directly connected the node (our method is graph-based).

The RC extraction method as presented here has been embedded in a prototype circuit extractor. Experiments have shown that the method indeed has a time complexity of $O(N)$, where N is the number of contour edges in the design. They also have shown that the extracted RC models can efficiently and accurately model the electrical behavior of the interconnections.

Presently we are incorporating some heuristics to prevent worst-case behavior of the program and to reduce the number of elements (resistors, capacitors and nodes) in the final network by neglecting irrelevant detail. These heuristics include (1) merging of (terminal) nodes that are connected by a small resistance, (2) removing large resistances that are short-circuited by a low-resistivity path, (3) reconnecting small coupling capacitances to ground, and (4) retaining of strategic nodes on large conductors (power and ground lines, clock lines and large busses with many connections) in order to prevent the creation of complete resistance graphs on their terminal nodes. Such heuristics will ensure the linearity of our method as well as a low complexity of the extracted networks without compromising their accuracy.

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