A 780 × 800 μ m² Multichannel Digital Silicon Photomultiplier With Column-Parallel Time-to-Digital Converter and Basic Characterization

Shingo Mandai, Vishwas Jain, and Edoardo Charbon

Abstract—This paper presents a digital silicon photomultiplier (SiPM) partitioned in columns, whereas each column is connected to a column-parallel time-to-digital converter (TDC), in order to improve the timing resolution of single-photon detection. By reducing the number of pixels per TDC using a sharing scheme with three TDCs per column, the pixel-to-pixel skew is reduced. We report the basic characterization of the SiPM, comprising 416 single-photon avalanche diodes (SPADs); the characterization includes photon detection probability, dark count rate, afterpulsing, and crosstalk. We achieved 264-ps full-width at half maximum timing resolution of single-photon detection using a 48-fold column-parallel TDC with a temporal resolution of 51.8 ps (least significant bit), fully integrated in standard complementary metal–oxide semiconductor technology.

Index Terms—Fluorescence lifetime imaging microscopy (FLIM), positron emission tomography (PET), silicon photomultiplier (SiPM), time of flight (TOF), time-to-digital converter (TDC).

I. INTRODUCTION

SILICON photomultiplier (SiPM) is an alternative to A photomultiplier tubes (PMTs) for the detection of highly localized (in time and space) bursts of photons associated with a physical phenomenon, such as a high-energy photon release or a laser pulse. SiPMs are often preferred to PMTs because of their tolerance to magnetic fields, compactness, and relatively low bias voltage [1]-[8]. Two flavors exist for SiPMs: analog and digital. An analog SiPM (A-SiPM) consists of an array of avalanche photodiodes operating in Geiger mode, also known as single-photon avalanche diodes (SPADs), whereas the avalanche currents are summed in one node as shown in Fig. 1(a), [1]–[7]. The resulting current is proportional to the number of detected photons, thus providing single- and multiple-photon detection capability. A digital SiPM (D-SiPM) is a device where each photodetecting cell is a SPAD whose voltage is combined digitally using an OR logical gate. Each SPAD is individually controlled to optimize overall dark counts and

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temporal response [8]-[12]. The output signal is a high-speed digital signal because all SPAD outputs are digital in nature and decoupled from each other until they reach the OR gate, as shown in Fig. 1(b). In most D-SiPMs, the global output is directly routed to an on-chip time-to-digital converter (TDC) to reduce external components and temporal noise. The time uncertainty for single-photon detection is limited by SPAD jitter and TDC nonlinearities, as well as systematic skews due to imperfectly balanced routing. A-SiPMs are especially sensitive to the systematic skews, while in D-SiPMs, the skews can be largely removed or compensated for. Alternatively, the approach pursued in [13] can achieve perfectly balanced routing by implementing an on-pixel TDC as shown in Fig. 1(c). Furthermore, the statistical approach to estimate time of arrival is possible for multiple-photon detection, whenever a scintillation or other photon generation process is used. The main drawback of the approach proposed in [13] is the low fill factor due to the need for significant silicon real estate to implement per-pixel functionality. Sharing several detector cells with one TDC has the advantage of increasing the fill factor while still enabling a somewhat independent photon time-of-arrival evaluation, as shown in Fig. 1(d). The skew problem is also improved when compared to conventional D-SiPMs for single-photon detection, and the multiple timing information can be utilized in a statistical approach for multiple-photon detection [14]-[16]. Fishburn and Seifert [14], [15] show the theoretical advantage of acquiring multiple timestamps for a TOF PET application and [16] shows that D-SiPMs utilizing multiple timestamps can be more tolerant to DCR than those utilizing a single timestamp. In this paper, we present a multichannel digital SiPM (MD-SiPM) with an array of 48 TDCs, each with a temporal resolution of 51.8 ps (LSB). This arrangement, known as column-parallel TDC, not only reduces the number of detector cells per TDC but also enables the characterization of the photon burst in terms of the first multiple photons impinging on the SiPM. Each TDC is shared by 8 or 9 SPADs in the SiPM. We report the basic characterization, including photon detection probability (PDP), dark count rate (DCR), afterpulsing, and crosstalk. The overall temporal accuracy for single-photon detection is 264 ps (FWHM), when the photon source exhibits 34 ps (FWHM) jitter. Both fine timing resolution and medium fill factor are achieved.

This paper is organized as follows. In Section II, the principle of the proposed MD-SiPM is presented. We de-

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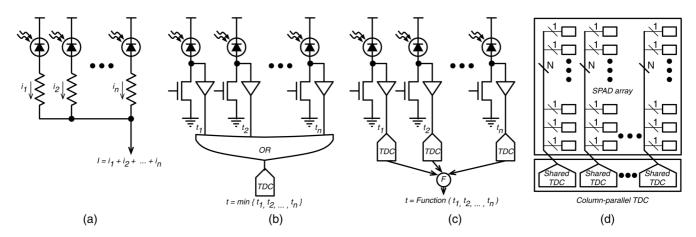


Fig. 1. Concept of (a) analog SiPM, (b) conventional digital SiPM, (c) digital SiPM with on-pixel TDC, and (d) proposed multichannel digital SiPM.

scribe the architecture, the circuit design, and the operation in Section III. In Section IV, the performance of the SPAD and SiPM is shown. The timing information with a single-photon scheme is also measured. Finally, a conclusion is presented in Section V.

II. MULTICHANNEL DIGITAL SIPM ARCHITECTURE

Fig. 2(a) shows the block diagram of the MD-SiPM [17]; it consists of an array of 16×26 photodetecting cells (called pixels hereafter), a 48-fold column-parallel TDC, precharge circuits, a row decoder, a mask register, and an energy register. The size of the MD-SiPM is 780 μ m \times 800 μ m. The pixel size is 30 μ m × 50 μ m with a 21.2% fill factor. The size of one TDC is 16 μ m \times 800 μ m, including the TDC data readout circuit, which is smaller than the already published column-parallel TDC [18]. In one column, three TDCs are implemented (to reduce the number of pixels per TDC) in an interlaced configuration. A mask register is used for disabling the pixels with DCR exceeding a threshold, in order to minimize spurious TDC activation. In our case, 15% of SPADs are masked for the timing characterization of the MD-SiPM. The energy register is used for reading out the detected photon information in order to calculate the total number of detected photons. The total number of detected photons corresponds to the radiation energy of a detected gamma ray and it is utilized in a PET to suppress spurious photons. Fig. 2(b) and (c) shows the microphotograph of the MD-SiPM and of the TDC, respectively.

III. CIRCUIT DESIGN

A. Pixel Configuration

Fig. 3(a) shows the schematic of a pixel circuit. The pixel comprises the SPAD [19], an active recharge circuitry to control dead time, a 2-b counter, a memory, and a masking circuit. Fig. 3(b) and (c) shows the timing diagram of the pixel operation. When photons are detected from, for example, a scintillator, the first photon generates a pulse that controls the TDC input line via a pull-down transistor. The dead time of a SPAD is controlled by DBIAS from 2.5 ns to infinity, and the 2-b counter counts how many photons or dark counts are de-

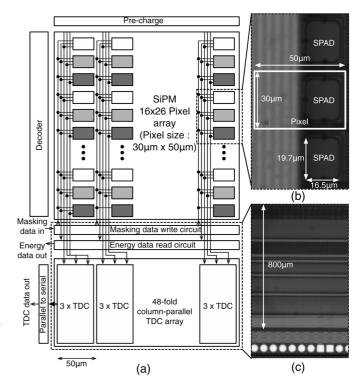


Fig. 2. (a) Sensor block diagram. (b) Detail of SiPM photodetector cells. (c) Column-parallel TDC microphotograph.

tected by the SPAD. QBIAS is zero to disable passive recharge when MD-SiPM is detecting a gamma ray. QBIAS is activated only for test purposes. The active recharge circuitry is disabled after the 2-b counter counts two photons not to recharge the SPAD by the third photon and to keep the counter values. In total, this MD-SiPM can count 1248 SPAD firings, which is 3 times the number of pixels, 416. The MD-SiPM is activated until the number of firing TDCs exceeds a threshold within a predetermined time, say 100 ns; otherwise, it is corrected every predetermined time. The output of the 2-b counter is saved to an on-pixel 2-b memory, and read out before the next frame. The 2-b memory data in each row are sent to the energy data readout circuit and read out outside the chip. The total readout time of the energy information is 9.88 μ s. ROWCALSEL is

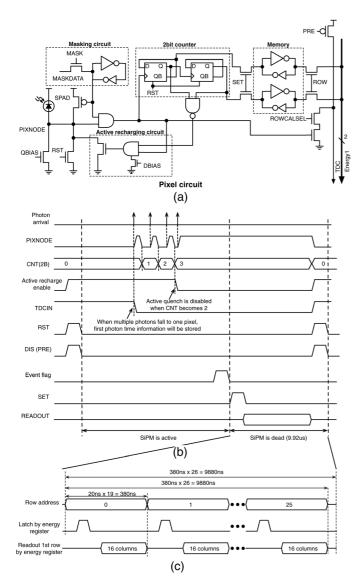


Fig. 3. (a) Schematic of pixel circuit. (b) Timing diagram of the pixel operation. (c) Timing diagram of energy readout from pixels in the MD-SiPM.

always on, except during calibration of DCR that is carried out in advance to check which SPADs should be masked. TDCs are also calibrated at the same time to measure system offset between TDCs due to routing unbalance. The masking circuit disables the SPADs with a DCR above a certain programmable threshold. Fig. 4 shows a tradeoff between the number of countable photons and fill factor. Fill factor becomes small when a pixel has a large number of bits for the counter and memory [Fig. 4(a)], while fill factor becomes big when a pixel has a small number of bits for the counter and memory [Fig. 4(a)]. Fig. 4(c) shows a tradeoff between fill factor and the maximum countable photons in each number of bits for the counter and memory. In our current complementary metal-oxide semiconductor (CMOS) process (0.35- μ m CMOS), it is difficult to achieve high fill factor and the high number of countable photons. However, this tradeoff can be solved by employing an advanced CMOS process, such as 130-nm CMOS, to reduce the area of circuitry.

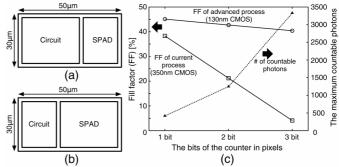


Fig. 4. (a) Pixel circuit with larger circuity, such as 3 b counter and memory. (b) Pixel circuit with smaller circuity, such as 1 b counter and memory. (c) Tradeoff between fill factor and the maximum countable photons.

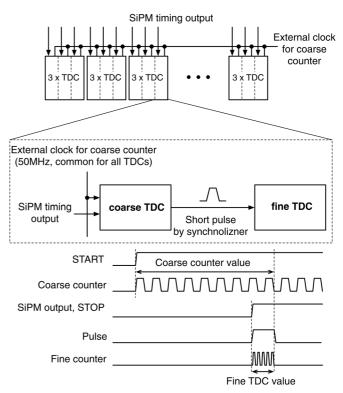


Fig. 5. TDC concept and operation.

B. TDC Configuration

Fig. 5 shows the TDC concept and timing diagram. The TDC comprises a coarse and fine conversion. The coarse clock CLK (50 MHz) is supplied from outside the chip and a coarse counter counts the clock cycles after a new frame starts. The coarse counter stops counting when STOP becomes high when a SPAD fires, and the synchronizer generates a pulse according to the time residue between CLK and STOP. The pulse corresponding to the time residue of the coarse TDC, EN, activates the fine TDC and starts the oscillation. During the pulse, the fine counter counts the oscillation cycles and the phase detector detects the phase when the oscillation stops.

Fig. 6(a) shows the schematic of the coarse TDC. The coarse TDC consists of a 10-b coarse counter and synchronizer. The synchronizer is composed of a serial connection of two D flip-flops and generates a pulse for the fine TDC. As shown in Fig. 6,

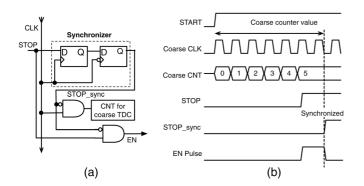


Fig. 6. (a) Structure of the coarse TDC. (b) Timing diagram.

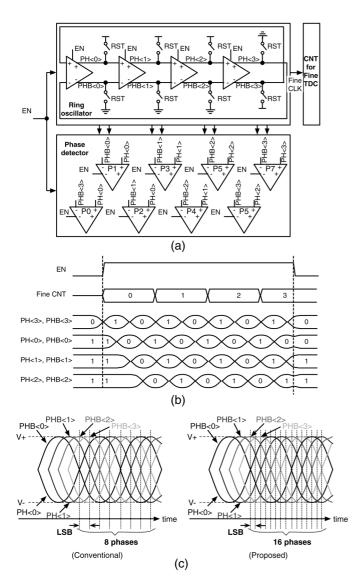


Fig. 7. (a) Structure of the fine TDC. (b) Timing diagram. (c) Concept of our proposed phase detector.

the coarse counter value keeps increasing until STOP becomes high. The EN signal for the fine TDC is generated by the XOR gate with STOP and the synchronizer output STOP_sync.

Fig. 7(a) shows the schematic of the fine TDC. The fine TDC consists of a 4-stage differential ring oscillator, a phase detector,

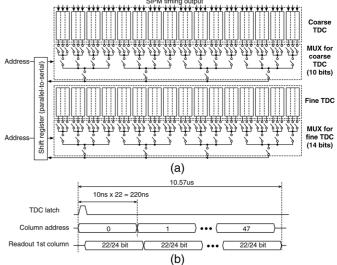


Fig. 8. (a) Structure of the TDC data readout circuit and (b) its timing diagram.

and a 6-b counter. The ring oscillator is reset by RST, and EN starts the oscillation, then the 6 b counter counts the cycle of the oscillation as shown in Fig. 7(b). Fig. 7(c) explains the difference between the conventional phase detector and our proposed phase detector. Conventionally, the phase detector looks at only PH(0) and PHB(0), PH(1) and PHB(1), PH(2) and PHB(2), and PH(3) and PHB(3), resulting in eight phases in one oscillation cycle. The LSB corresponds to one over eight of the oscillation periods. However, our proposed phase detector employs an interpolation technique to double the phase resolution, thus halving the LSB. By expanding the comparison to $PH\langle 0 \rangle$ and PHB(3), PH(0) and PHB(1), PH(1) and PHB(2), and PH(2)and PHB $\langle 3 \rangle$, the interpolated phase is detectable, as shown in Fig. 7(c). Only four extra comparators and memory are required. Finally, the coarse TDC data and the fine TDC data are summed up to achieve 19 b resolution.

Fig. 8(a) shows the structure of the TDC data readout circuit. Two multiplexers (MUX) are implemented for the coarse and fine TDC. After the address is set to a target column of TDCs, the output from the multiplexers is sent to a shift register to be read out outside the chip. Fig. 8(b) shows a timing diagram to read out 48 TDC data. In total, it takes 10.57 μ s to read out all 48 TDC data.

C. MD-SiPM Operation

Fig. 9 shows the MD-SiPM flowchart. First, the MD-SiPM starts to write mask information to the mask register, and masking of noisy pixels is carried out. After the masking, the MD-SiPM is ready for detecting gamma rays by setting the Event flag to zero. When MD-SiPM receives a gamma ray, the number of firing TDCs exceeds the threshold (TH_{tdc}) and the Event flag becomes one. After a fixed period (60 ns – 5 μ s), all TDCs and pixels are refreshed in 40 ns if the Event flag is zero and the next frame starts. If the Event flag is one, all TDCs and pixels are read out outside the chip in parallel in 10.57 μ s, and

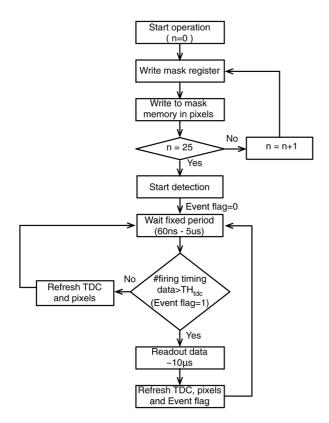


Fig. 9. Flowchart of the MD-SiPM operation.

the next frame starts after reseting all TDCs, pixels, and Event flag.

IV. MEASUREMENT RESULTS

A. TDC Characterization

We have designed and fabricated the MD-SiPM using a $0.35 \ \mu m$ high-voltage CMOS process. The power-supply voltage is 3.3 V. The TDCs are characterized at room temperature by operating all TDCs at the same time in a photon-starved regime. Fig. 10(a) and (b) shows the differential nonlinearity (DNL) and integral nonlinearity (INL) of one particular TDC in the 260 ns input range, respectively, which was acquired by density test; the SPAD is used to generate random STOP signals for the TDCs [20]. The LSB is 51.8 ps and the average of the worst case DNL and INL in 48 TDCs is 1.97 LSB and 7.18 LSB, respectively. INL can be compensated to 2.39 LSB which is the average of the worst case INL using a lookup table made in advance because the INL is systematic variation. The lookup table is implemented, and the final TDC value is processed on the host PC. The worst INL variation of 48 TDCs before INL compensation and after INL compensation is shown in Fig. 10(c). TDC intrinsic jitter at 93.2 ps (timing uncertainty) is also observed utilizing an electrical STOP signal from outside the chip. The jitter is acceptable while worst-case DNL is more than 1 considering that the scintillator has worse timing uncertainty in a PET application (conventionally more than 200 ps with reasonable crystal length).

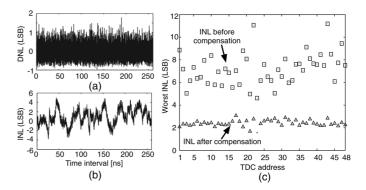


Fig. 10. TDC measurement results of (a) DNL and (b) INL. (c) INL variation in 48 TDCs before INL compensation and after compensation.

B. Single-Photon Avalanche Diode Characterization

The SPAD geometry is a rounded rectangle to prevent electrical-field nonuniformity around corners of the SPAD. Breakdown voltage was observed to vary from 19.1 to 19.4 V at 20 °C. Other than process variations, the breakdown voltage also depends on temperature with an increase of 0.2 V every 10 °C. To measure the sensitivity of the SPAD, the light from a monochromator (Oriel/Newport part 77250) was projected into an integration sphere (Oriel/Newport part 819D-SL-2) with a reference diode (Hamamatsu part S1226-BQ) at one port of the sphere and the SPAD at the other. With the integration sphere, the amount of photons is identical for the reference diode and the SPAD, and by decreasing the intensity of the light source, the SPAD works with the single-photon regime. A SPAD's sensitivity to incident photons is characterized by the photon detection probability (PDP) that quantifies the probabilities that a photon impinging on the detection triggers a digital response. When the PDP is measured, the afterpulsing, which is an unwanted avalanche triggered by trapped carriers released during the SPAD's recharge, should be negligible not to overestimate the PDP. It means that the deadtime of the SPAD, which is the time to restore the anode voltage to the excess bias after the SPAD has an avalanche, is set to be long by using a high quenching resistor by enabling QBIAS, in this case, 200 ns. Fig. 11(a) shows PDP measurement results for different wavelengths. The temperature dependency of PDP is negligible in the spectral range of interest for this project. PDP is about 30% at 4 V excess bias at a 420–430 nm wavelength, which is of interest for TOF PET applications with LYSO:Ce (LYSO) scintillators.

DCR measurement is carried out in the dark where the chip is shielded completely from light. The DCR is measured by acquiring the probability of avalanche in a fixed period, T in our case, 270 ns, while the SPAD is operating at a given excess bias. By counting the number of avalanches by iterating 25 600 times, the DCR probability $P_{\rm dcr}$ can be acquired accurately. The probability is equal to $1 - e^{-DCR \times T}$ because the avalanche follows a Poisson distribution. Thus, DCR is calculated using the acquired possibility as follows:

$$DCR = \frac{1}{T} \times \ln\left(\frac{1}{1 - P_{dcr}}\right).$$

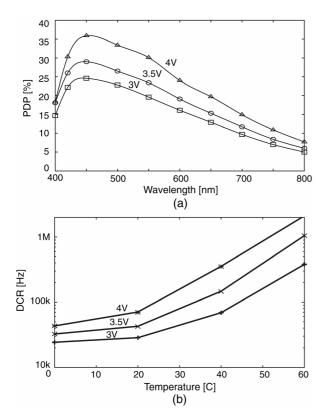


Fig. 11. (a) PDP and (b) DCR characterization in various excess bias voltages.

Fig. 11(b) shows DCR measurement results for various excess bias voltages (3 to 4 V) and temperatures (0 to 60° C). The DCR values are the median of all 416 SPADs DCR values in the MD-SiPM.

Under constant light intensity, the distribution of times between a SPAD's avalanches, or interavalanche times, should follow the Poisson statistics. An afterpulse is an unwanted avalanche triggered by trapped carriers released during the SPAD's recharge time. As a result, a SPAD's count distribution for each interavalache time does not follow a pure exponential curve, and the afterpulsing probability can be calculated by summing the counts in an interavalanche time histogram above an exponential line fitted to infinite interavalanche times or, in practice, larger than a value of roughly 50 μ s, as shown in Fig. 12(a). Then, the afterpulsing probablity is calculated by dividing the summed counts above the fitted exponential line by the total counts until 50 μ s. Fig. 12(b) shows the afterpulsing probability at various deadtimes, Afterpulsing and finite deadtime cause miscounting and overcounting, which affect the photon counting accuracy of the MD-SiPM.

C. SPAD Array Characterization in the SiPM

The cumulative DCR for the integrated 416 SPADs in the MD-SiPM is plotted in Fig. 13. Fig. 13(a) and (b) shows temperature and excess bias voltage variations of cumulative DCR. Noisy SPADs are roughly 15% in each condition before masking. This relatively high percentage is due to the use of a standard CMOS process that was not optimized for SPADs. Fig. 14 shows chip-to-chip variation of a DCR in the MD-SiPM. It is to be observed that noisy pixels are distributed

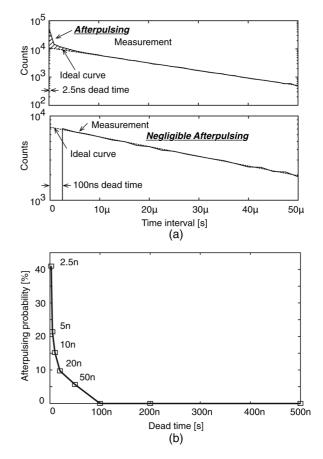


Fig. 12. Afterpulsing: (a) histogram of interavalanche times measured at the output of a pixel and (b) afterpulsing probability as a function of deadtime.

at random in the entire MD-SiPM, and the ratio of noisy SPADs per MD-SiPM is constant and independent of temperature, excess bias, and chip-to-chip variations.

D. Crosstalk

By using the masking circuitry, optical and electrical crosstalk is measured. Fig. 15 shows the DCR map at 4 V excess bias, 30°C temperature in a section of the MD-SiPM that contains a noisy pixel before (a) and after (b) masking of pixels whose DCR is higher than 1 MHz. Fig. 15 also shows the DCR reduction in pixels surrounding the noisy SPAD in 4×4 pixels. The crosstalk is calculated by summing up each DCR of these 16 pixels before and after turning off the noisy pixel, and then calculating a reduction ratio from DCR summations before and after turning the SPAD off. By turning off the noisy pixel, DCR decreases approximately 10% in adjacent pixels.

E. Single-Photon Detection

The whole MD-SiPM is illuminated by a picosecond laser diode source emitting 34 ps pulses at a 40 MHz repetition rate with 405 nm of wavelength (Advanced Laser Diode Systems GmBH, Berlin, Germany). Fig. 16(a) shows measurements of time resolution of the MD-SiPM for a single-photon mode. The single-photon timing resolution of the MD-SiPM is measured with a single-photon level intensity obtained from a laser on average. Asymmetric shape of the count level before and after

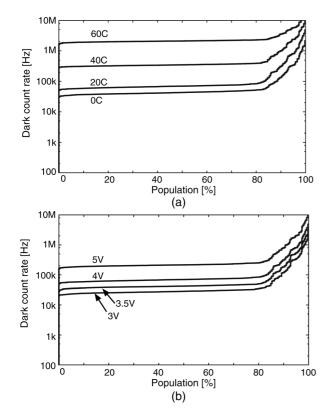


Fig. 13. Cumulative DCR plot for the MD-SiPM. (a) Temperature dependence at 4 V excess bias. (b) Excess bias dependence at 20 $^{\circ}$ C.

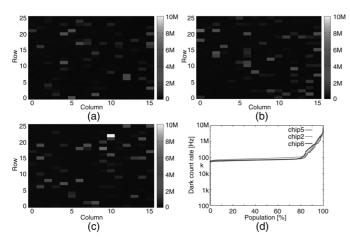


Fig. 14. DCR map of (a) Chip1, (b) Chip 2, and (c) Chip3. (d) Cumulative DCR plot of three different chips.

the laser pulse is due to the fact that a laser intensity is close to one photon per laser pulse and the relatively high DCR will trigger the MD-SiPM before but not after the laser pulse. The timing resolution for the single-photon mode consists of mainly SPAD jitter, TDC intrinsic jitter, pixel-to-pixel skew of the TDC input lines, and laser jitter. The FWHM timing resolution is 264 ps including the SPAD jitter, 93.2 ps TDC intrinsic jitter, and the pixel-to-pixel skew when the photon source exhibits 34 ps FWHM jitter at 3 V excess bias. Fig. 16(b) shows the FWHM timing resolution as a function of excess bias. The timing resolution improves by increasing excess bias for SPADs, because the SPAD jitter dramatically decreases

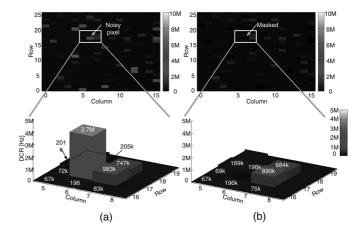


Fig. 15. DCR map (a) before masking a noisy SPAD and (b) after masking a noisy SPAD. The values in the bottom pictures show the DCR.

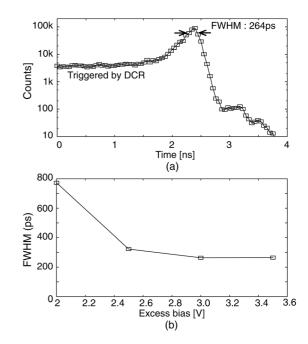


Fig. 16. (a) Measurement results of time resolution for a single photon. (b) Time resolution as a function of excess bias.

when the excess bias is high. Table I summarizes the performance of our detector in comparison with other SiPMs found in the literature. The comparison is based on one SiPM [1] or pixel [9], [12]. We obtained a lower temporal uncertainty for single-photon detection than previously reported digital SiPMs [8], while achieving a relatively high fill factor of 21.2%. By utilizing an advanced CMOS process, such as [12], the timing performance and the fill factor can be improved dramatically.

F. Coincident Timing Resolution Prediction

To predict the coincident timing resolution (CTR) based on the MD-SiPM architecture and measurement data shown in the previous subsections, we carried out a simulation [22]. For our simulations, we assumed normal SPAD jitter and electrical jitter distributions with an FWHM of 264 ps, and the rise and decay times of an LYSO scintillator are 100 ps and 40 ns, respectively. The detection probability density function

Parameter	Our work	[1]	[8], [9]	[12]
Tech.	multi digital	analog	digital	digital
Area (mm ²)	0.8x0.78	1x1	3.9x3.2	0.61x0.57
# SiPM	1	1	4	128
Fill factor(%)	21.2	30-78	54/74	42.93
# TDC per SiPM	48	0	2	2
LSB (ps)	51.8	-	24	63.9
Time res. @1 ph(ps)	264	190 [21]	>350*	265.7

* The data are calculated with the equations proposed in [8].

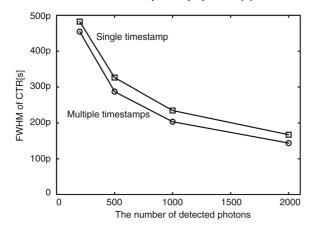


Fig. 17. Predicted CTR (FWHM) as a function of detected photons using single and multiple timestamps.

is used for calculating the Fisher information [15], [23] for the rth-order statistics pdf or the joint pdf for the first r-order statistics, then the Crámer–Rao lower bound for the unbiased estimator is calculated. Fig. 17 shows the relation between the number of detected photons and the predicted FWHM of CTR utilizing a single timestamp or multiple timestamps. According to the simulation results, the predicted CTR for the MD-SiPMs with 264 ps single-photon timing jitter will be 287 ps and 203 ps for 500 and 1000 photons, respectively, by utilizing multiple timestamps. CTR utilizing multiple timestamps does not degrade due to DCR while CTR utilizing a single timestamp degrades with certain values of DCR.

V. CONCLUSION

We have proposed a new type of SiPM, denominated MD-SiPM, based on column-parallel TDCs, in order to improve the time resolution of single-photon detection and multiple-photon detection through statistical approaches. By reducing the number of pixels per TDC, the pixel-to-pixel skew is reduced. We reported the basic characterization of a SPAD and an SiPM composed of 416 SPADs, including PDP, DCR, afterpulsing, and crosstalk. We achieved 264 ps FWHM timing resolution of single-photon detection using a 48-fold column-parallel TDC with a temporal resolution of 51.8 ps (LSB), fully integrated in standard CMOS technology.

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